NICE2025, Heidelberg 2025-03-25

## 28nm Embedded RRAM for Consumer and Industrial Products: Enabling, Design, and Reliability

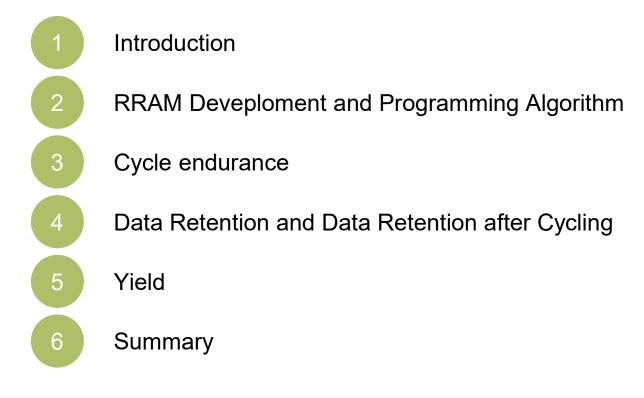
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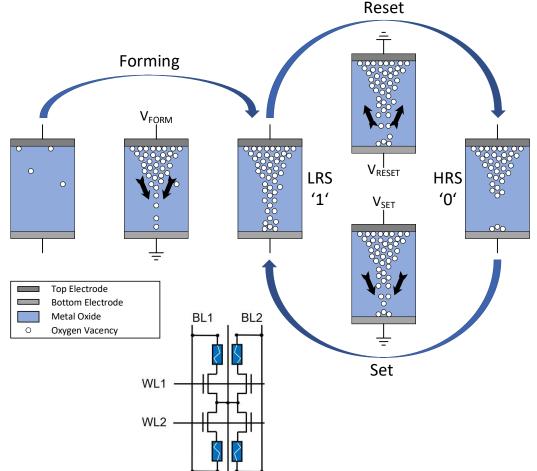
RRAM = Resistive Random Access Memory



Why a new non-volatile memory technology?	Why emerging memory in general?
for newer semiconductor technologies, embedded <b>Flash does not shrink well</b> , and	typically much lower wafer cost compared to corresponding embedded Flash
increased cost of Flash integration into advanced manufacturing processes	no impact on base technology enables reuse of existing circuits
What are the advantages of RRAM?	What are the challenges for RRAM?
Iowest cost of all emerging memories available at foundries	<ul> <li>potential issues with reliability:</li> <li>data retention at high T</li> <li>endurance</li> </ul>
it behaves like a (slow) RAM with retention and independent bit toggling → easy for SW	Flash know-how only partly reusable

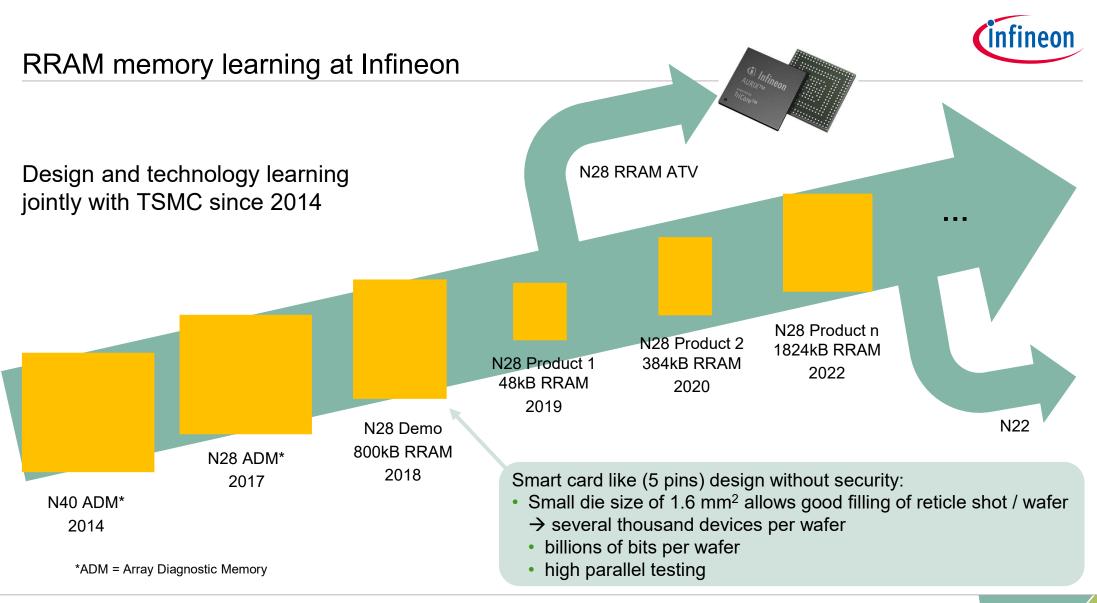


### RRAM – Physical Principle

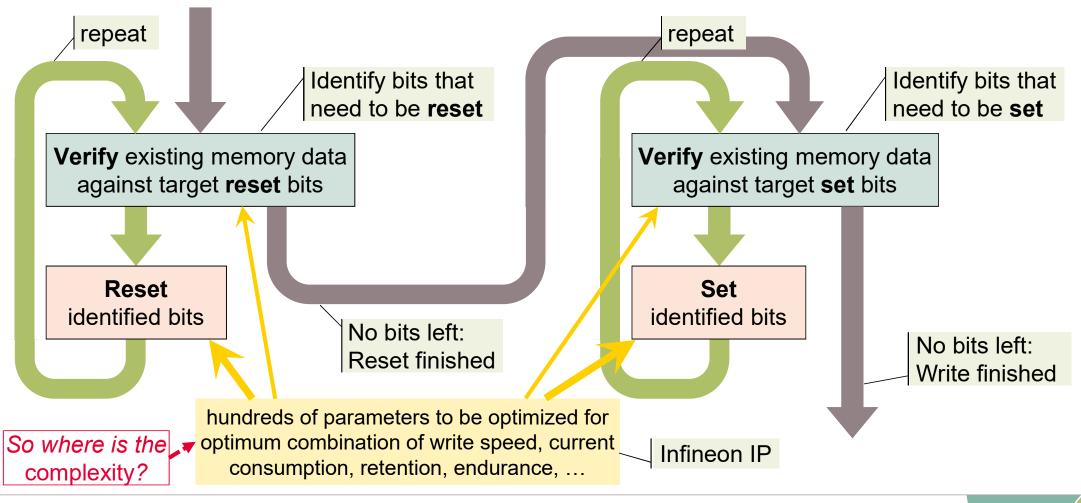


RRAM is based on a reversible soft breakdown:

- Forming operation creates conductive filament of Oxygen Vacancies
- Reset operation breaks the filament, resulting in a High Resistance State (HRS)
- Set operation recreates the filament, resulting in a Low Resistance State (LRS)
- RRAM cells located in backend of line between two metal layers, in place of vias
  - Very small number of extra mask layers
  - No extra temperature budget in frontend of line → no influence on base technology
- Memory elements: Combination of RRAM cells plus select transistors in 1T1R configurations, finally forming a memory field



# RRAM – Complex Iterative Write Algorithm in Hardware – Even for a Purely Digital Operation



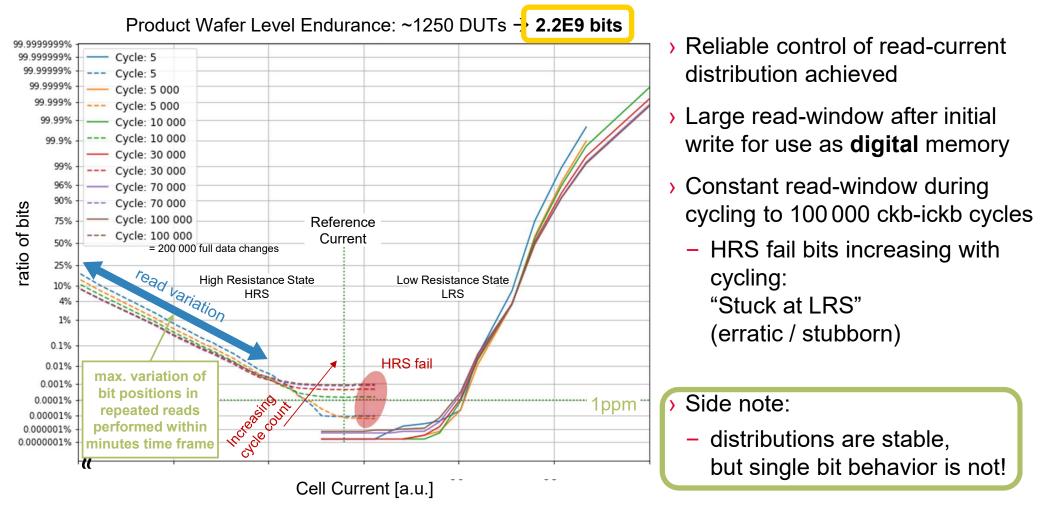
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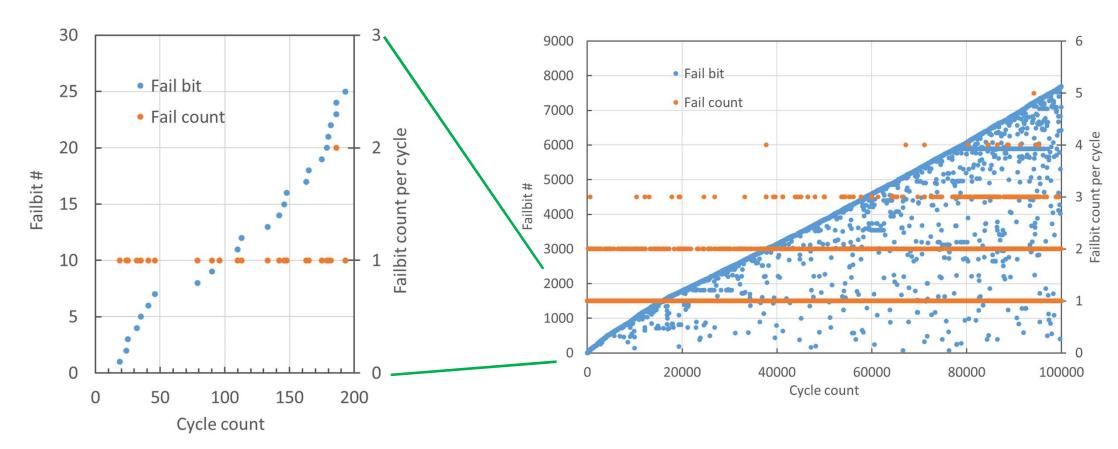


### RRAM 28nm – Endurance (Cycling) / Cell Current Distributions





### RRAM 28nm – Endurance (Cycling) / Erratic Bit Occurrence



Almost 3% of cycled bits at least once show erratic behavior during 100 000 cycles endurance test
 → Need suitable error correcting code (ECC) to cover erratic and stubborn bits



#### RRAM 28nm – Full Wafer Data Retention @ T=175°C Product Wafer Level Bake: 5 wafers - ~3E11 bits $E_a = 1.65 \text{ eV}$ extracted from 99.99999999% All DUTs, Initial 99.9999999% 99.999999% All DUTs, Initial measurements, 99.99999% All DUTs, 9h bake but standard Arrhenius model not 99.9999% All DUTs, 9h bake 99.999% All DUTs, 12h bake fully fitting for RRAM 99.99% --- All DUTs, 12h bake 99.9% $\rightarrow$ New retention model developed 99% 96% → High $E_a \rightarrow 9$ h @175°C bake 90% ratio of bits Reference 75% equals ~25 years @85°C Current 50% **High Resistance State** Low Resistance State 25% I RS HRS 10% > Tilt of HRS- and parallel shift of 4% 1% LRS-distribution during bake 0.1% 0.01% 0.001% Additional stress to consider: 0.0001% 1ppm 0.00001% 0.000001% Soldering (260°C) 0.0000001% 0.00000001% Þ Chip assembly flow \_ Cell Current [a.u.]

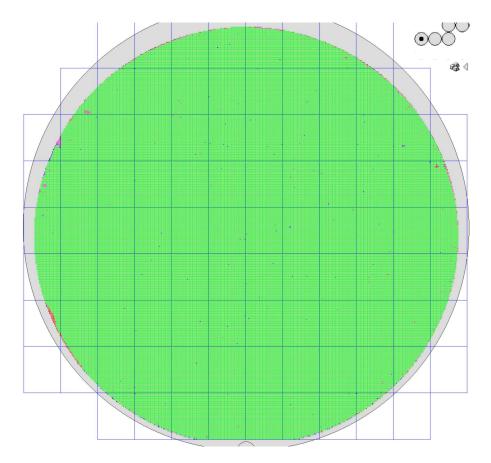


#### RRAM 28nm – Retention After Cycling (RAC) Wafer Level Endurance: ~1300 DUTs Good read window after cycling initial 99.99999% – – – initial and retention bake (RAC) 99.9999% - 2h bake 99.999% 100 000 pre-cycles - - 2h bake 99.99% initial, stuck bits removed 99.9% - - - initial, stuck bits removed $\rightarrow$ E<sub>a</sub> changes with cycling, 2h bake, stuck bits removed 99% bake of 2 h @175°C equals - - - 2h bake, stuck bits removed 96% 90% ~4 years @85°C ratio of bits 75% Reference 50% Current 25% > Side notes: 10% High Resistance State Low Resistance State 4% Also CAR (Cycling after HRS LRS 1% Retention) must be checked! 0.1% - All results depend on the 0.01% 0.001% used programming algorithm! 1ppm 0.0001% 0.00001% Cell Current [a.u.]

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### RRAM 28nm – Yield of Product Wafer

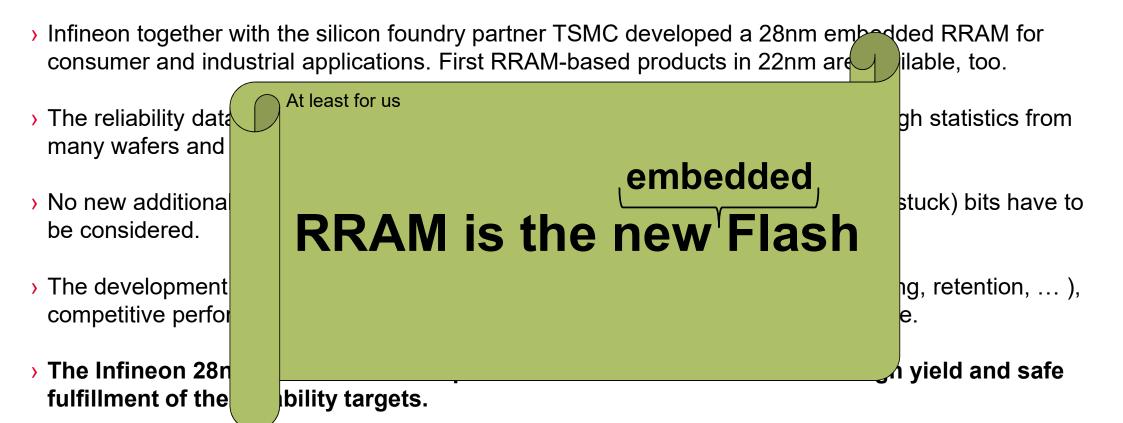


> 12" Wafer-map of 28nm product with 48kB embedded RRAM, overall product yield > 99 %

### Summary

- Infineon together with the silicon foundry partner TSMC developed a 28nm embedded RRAM for consumer and industrial applications. First RRAM-based products in 22nm are available, too.
- The reliability data is looking very good, not only on single DUT data but also on high statistics from many wafers and lots.
- No new additional failure modes were found for RRAM, only retention and erratic (stuck) bits have to be considered.
- The development of the programming algorithm is the key for good reliability (cycling, retention, ...), competitive performance and electrical parameters of the embedded RRAM module.
- The Infineon 28nm and 22nm RRAM products can be manufactured with high yield and safe fulfillment of the reliability targets.
- > Note: Infineon decided to use RRAM also in future high-end automotive microcontrollers.

### Summary



> Note: Infineon decided to use RRAM also in future high-end automotive microcontrollers.



### Links

### > Papers:

 C. Peters, F. Adler, K. Hofmann and J. Otterstedt, "Reliability of 28nm embedded RRAM for consumer and industrial products," *2022 IEEE International Memory Workshop (IMW)*, Dresden, Germany, 2022, pp. 1-3, doi: 10.1109/IMW52921.2022.9779300.

- N. Kopperberg et al., "Endurance of 2 Mbit Based BEOL Integrated ReRAM," in *IEEE Access*, vol. 10, pp. 122696-122705, 2022, doi: 10.1109/ACCESS.2022.3223657.
- Alessandro Grossi et. al.,
   "28nm Data Memory with Embedded RRAM Technology in Automotive Microcontrollers," 2023 IEEE International Memory Workshop (IMW), Monterey, US, 2023, pp. 1-4, doi: 10.1109/IMW56887.2023.10145951
- S. Wiefels et al.,
   "Reliability Aspects of 28 nm BEOL integrated ReRAM," in *physica status solidi (a) applications and materials science*, doi: 10.1002/pssa.202300401.
- ..
- > Press release:

"Infineon and TSMC to introduce RRAM technology for automotive AURIX™ TC4x product family", <a href="https://www.infineon.com/cms/en/about-infineon/press/market-news/2022/INFATV202211-031.html">https://www.infineon.com/cms/en/about-infineon/press/market-news/2022/INFATV202211-031.html</a>

Acknowledgment

> Many thanks are going to all the supporting colleagues from Infineon and TSMC.

Thank you for your attention!

Questions?



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