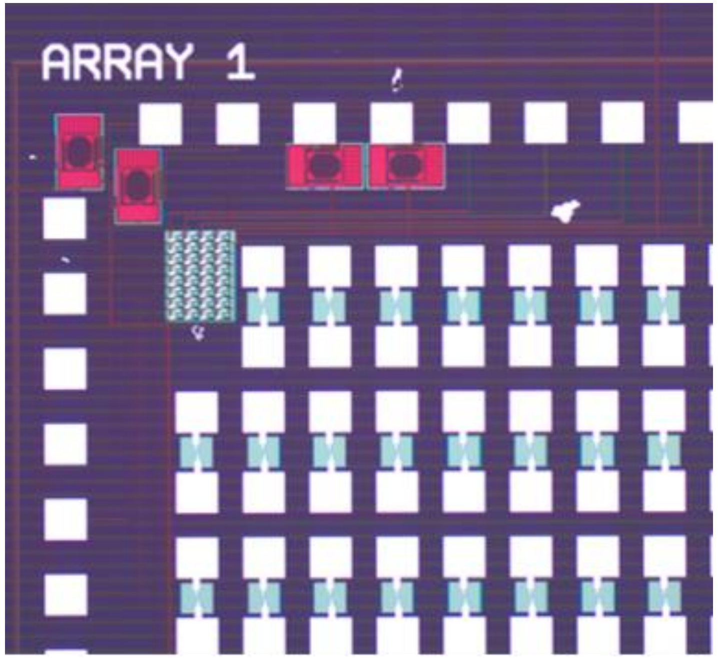
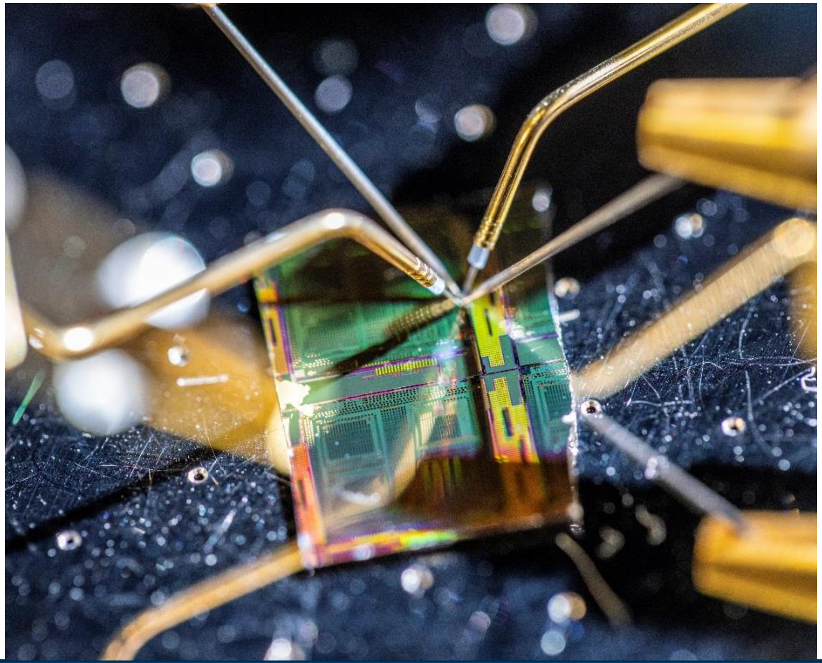
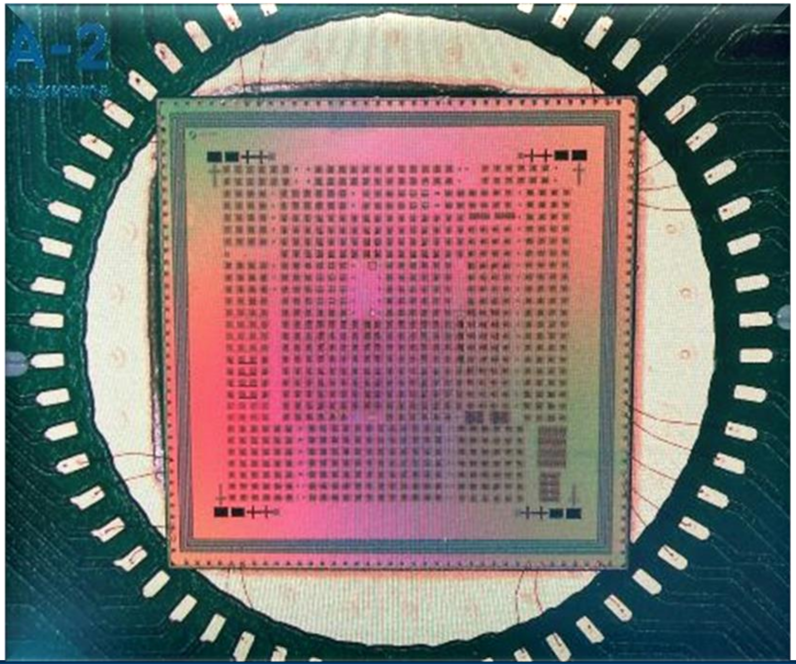






MEMRISTIVE VALENCE CHANGE MEMORY CROSS-BAR ARRAYS FOR NEUROMORPHIC COMPUTING

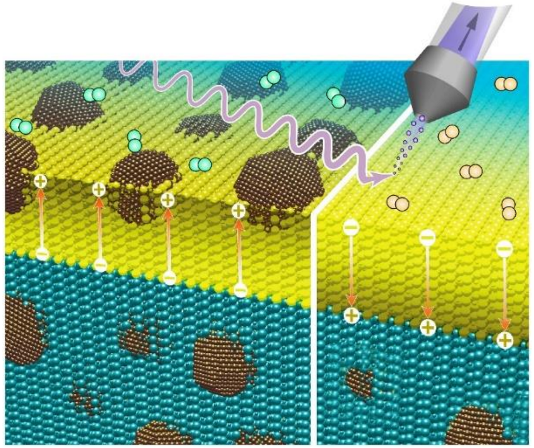
R. DITTMANN, S. WIEFELS, S. HOFFMANN-EIFERT, V. RANA, S. MENZEL
PGI 7, FORSCHUNGSZENTRUM JÜLICH GMBH

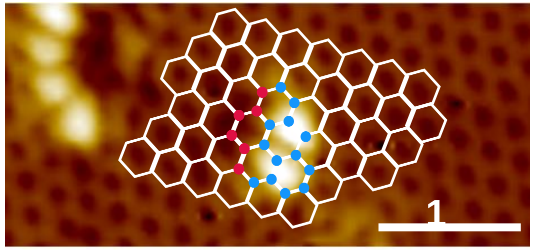
LUND UNIVERSITY

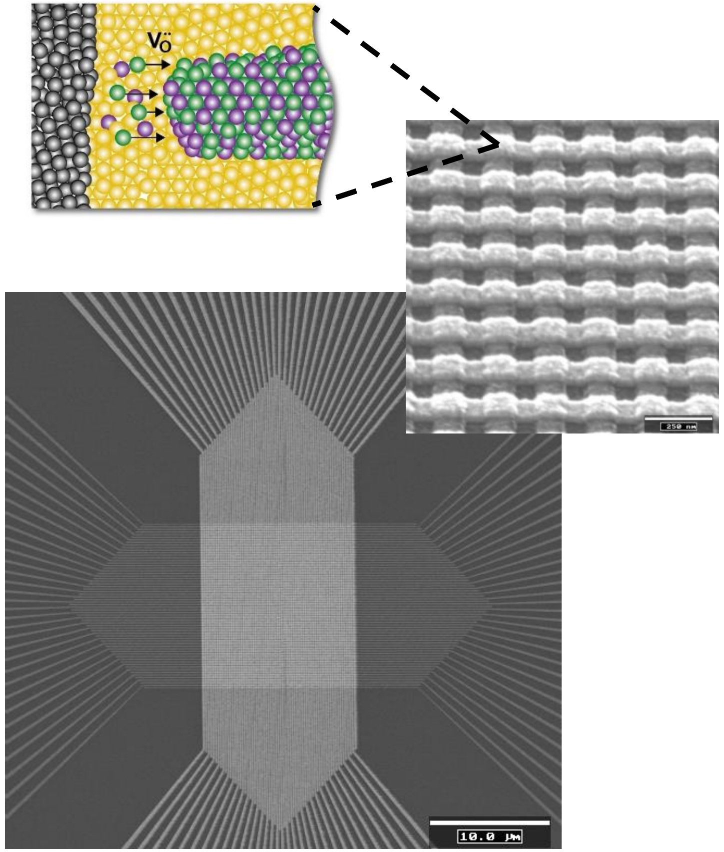
RWTH AACHEN UNIVERSITY

JÜLICH Forschungszentrum
Wandel gestalten

Institute of Electronic Materials @ FZ Jülich





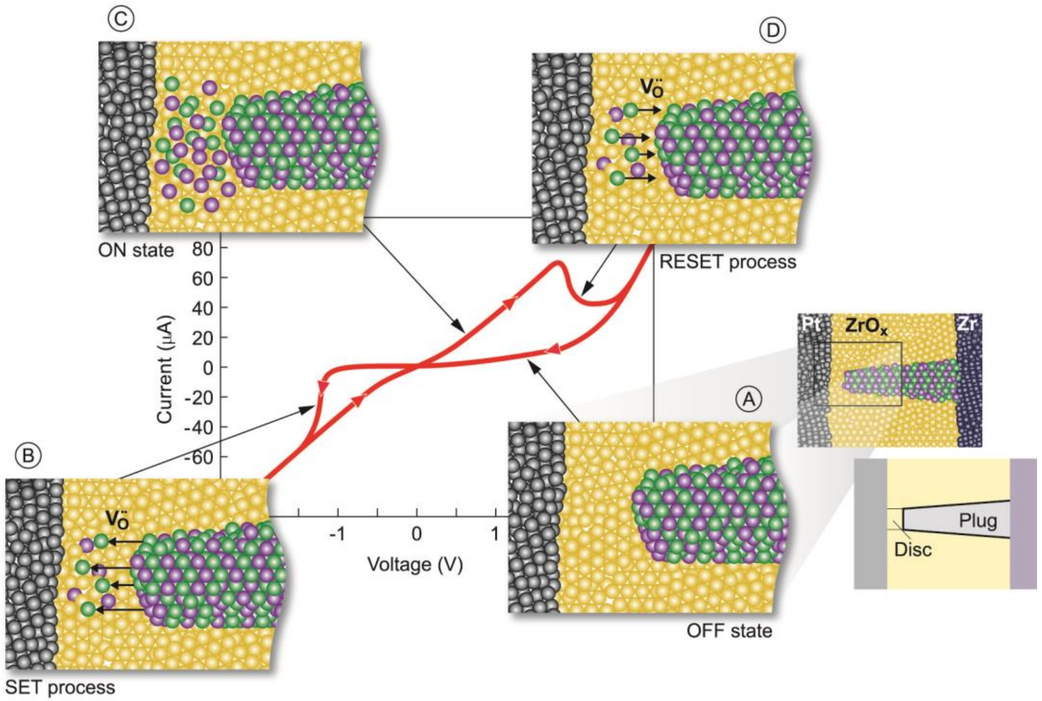


Materials and phenomena

Devices and integration technology

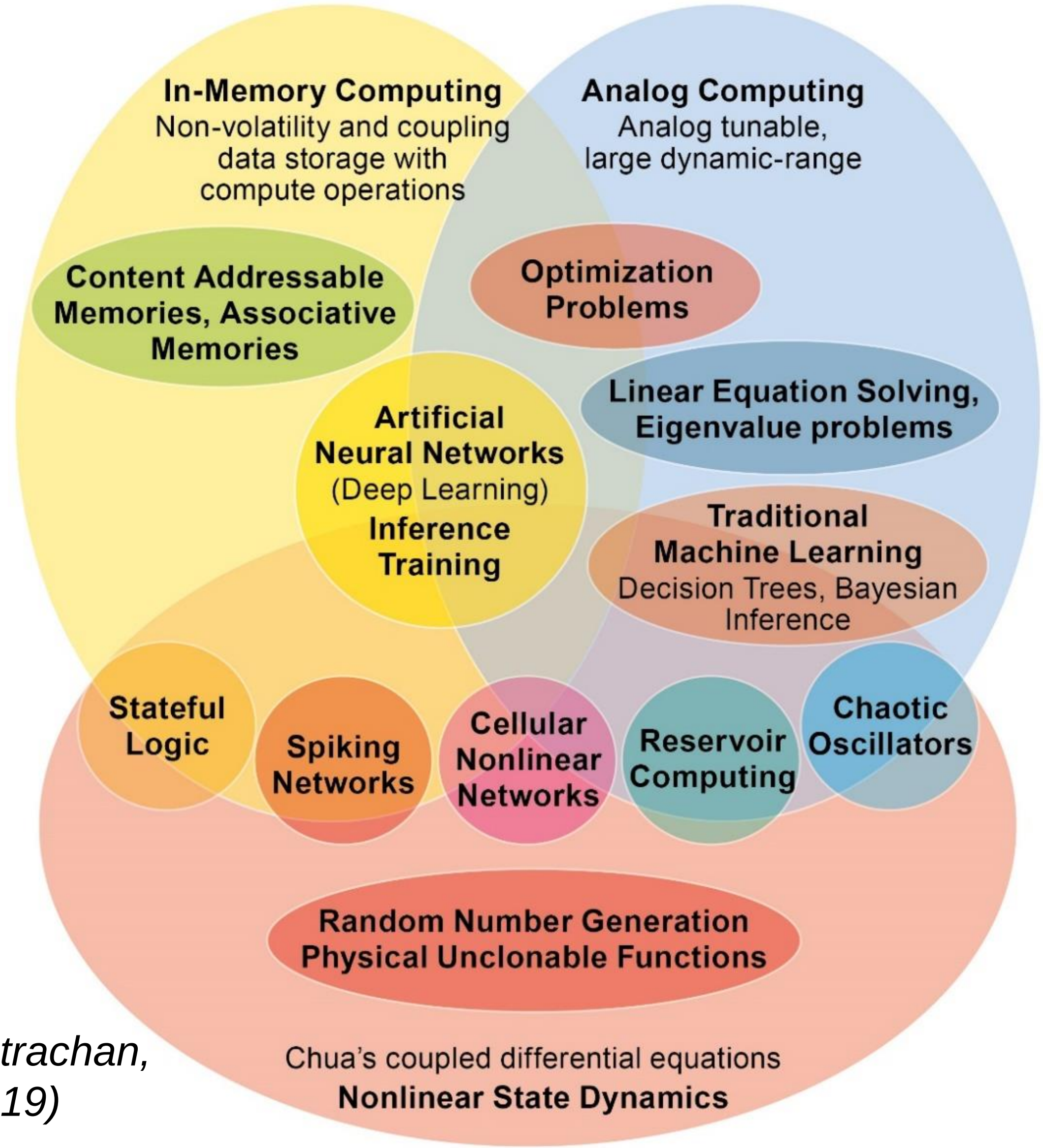
Memristive neuromorphic hardware

Valence change memory



R. Dittmann, St. Menzel, R. Waser, Adv. Physics (2023)

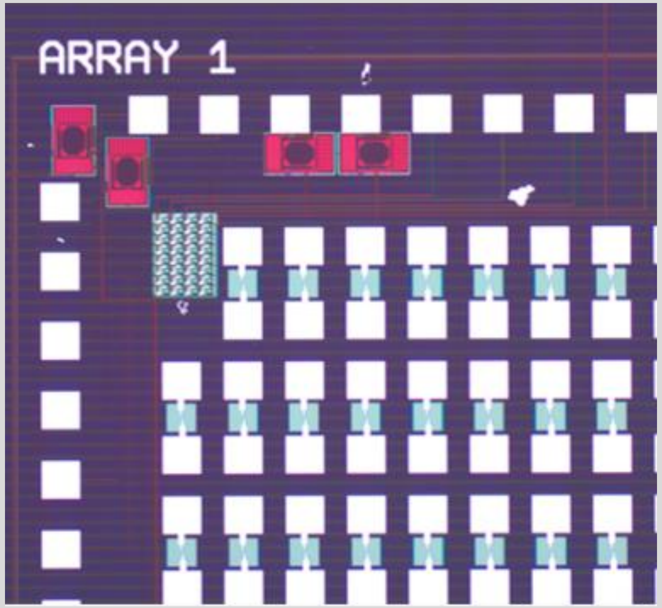
ReRAM: embedded non-volatile memory



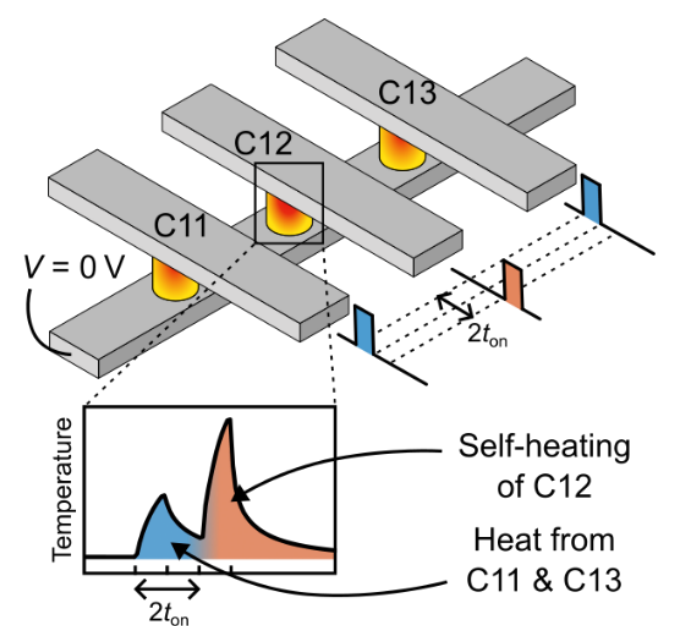
R. Dittmann, JP Strachan, APL materials (2019)

Outline

1T1R memristor cross-bar arrays

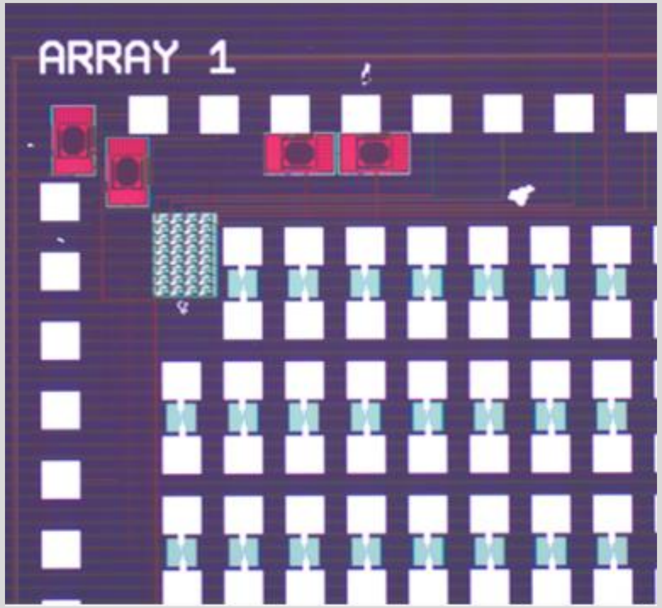


Spatio-temporal effects in cross-bar arrays

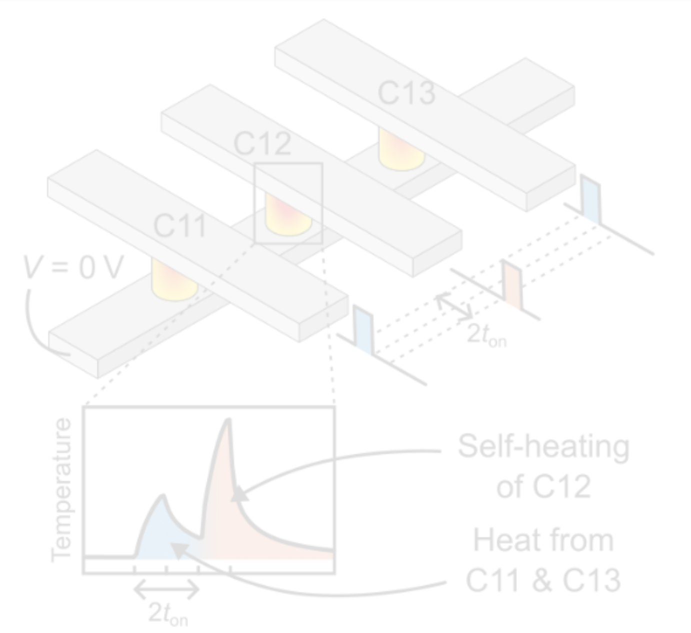


Outline

1T1R memristor cross-bar arrays

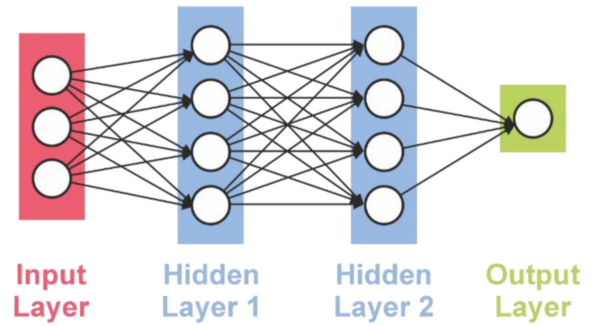


Spatio-temporal effects in cross-bar arrays



Applications of memristor cross-bar arrays

CMOS co-integrated memristor arrays are core blocks to serve many applications



Low-energy matrix multiplication "in-memory”

→ core operation of deep learning, signal processing, etc.

Spiking Neural Networks

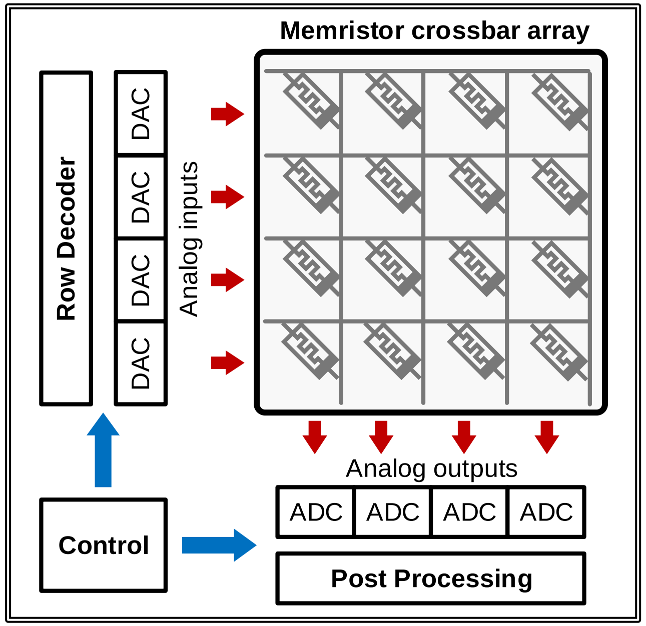
→ peripheral blocks for quasi-continuous time processing

Associative Memories / Content Addressable Memory

→ novel memory arrays addressed by content

RISC-V Processors and Network-on-Chip

→ flexible digital support and off-chip communication



NEUROTEC

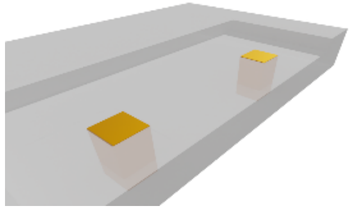
Cooperation:
Stefan van Waasen
John Paul Strachan
Emre Neftci

CMOS Co-integration

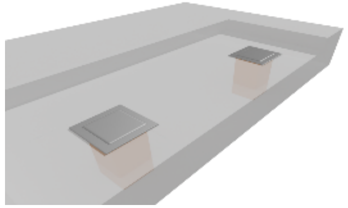
TSMC 28 nm technology (X-Fab 180nm)

Process flow

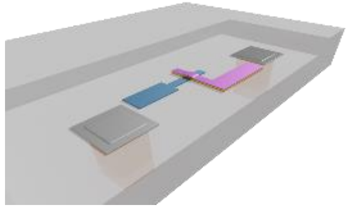
About 30 process steps in total



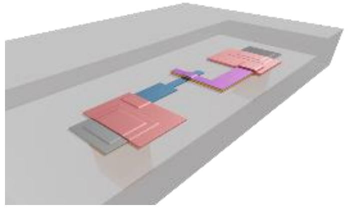
Opening of **metal contacts** to CMOS vias



Contact pad deposition



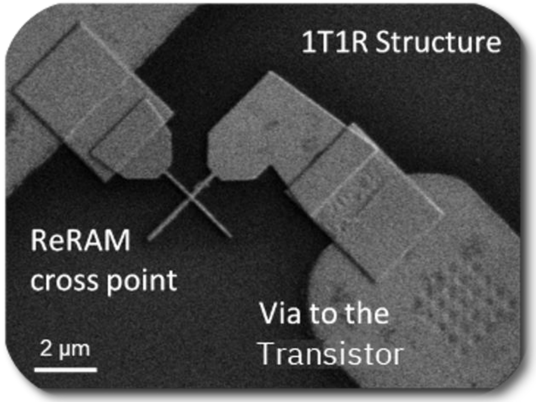
Memristive device fabrication as 100 nm x 100 nm crossbar



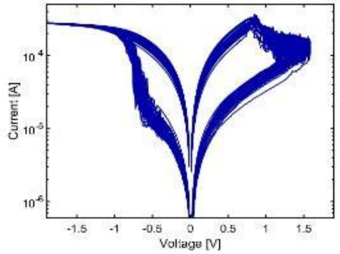
Connecting the memristive device with the contact pads to CMOS

Susanne Hoffmann-Eifert

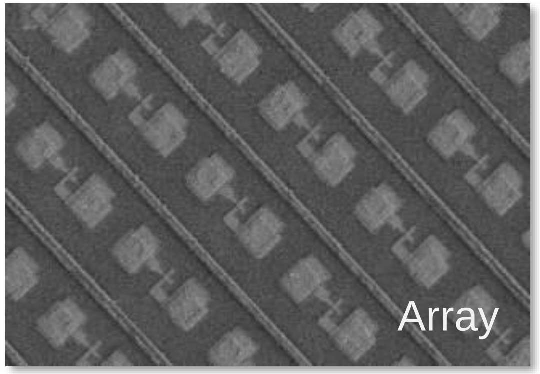
Delivered MPW Chips

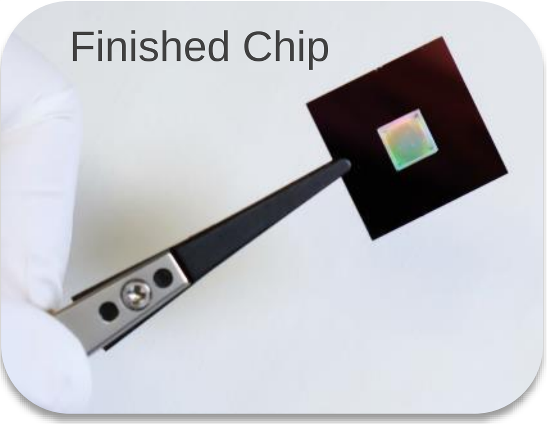


Pt/Ta/Ta_2O_5/Pt



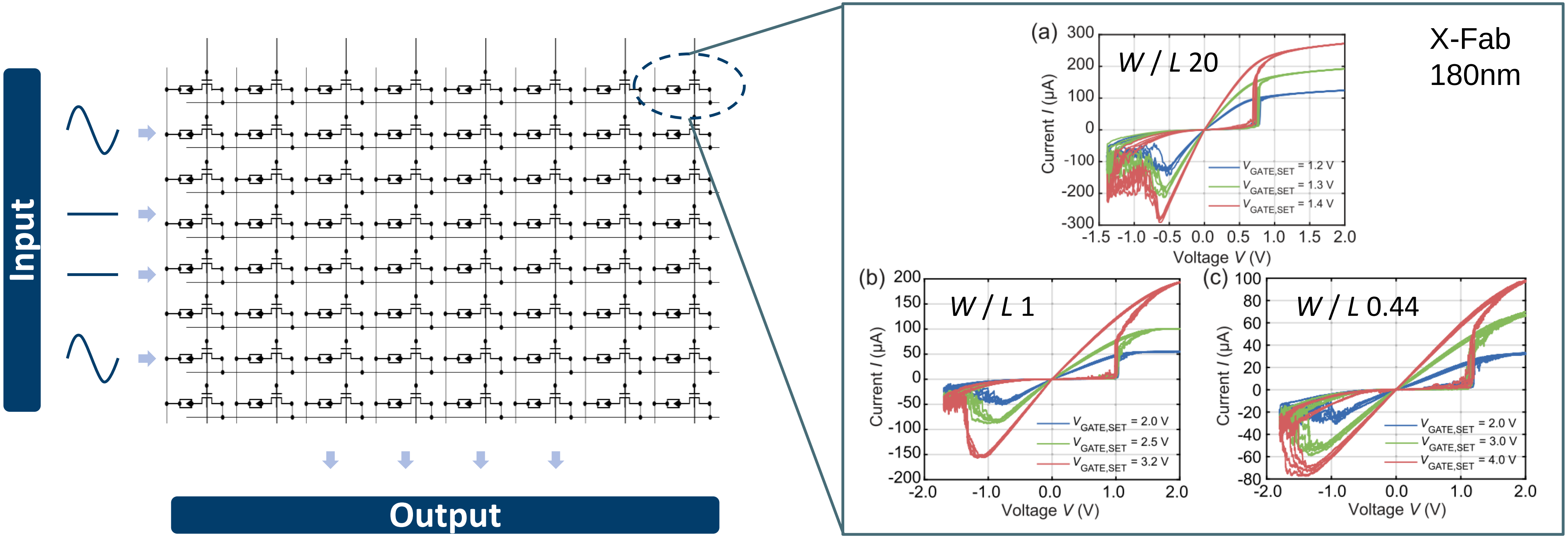
Reference sample on NEUROTEC-1 chip





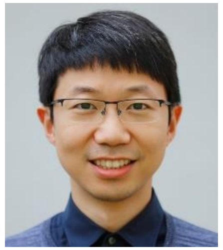
Collaboration AMO GmbH

Interplay between transistors and ReRAM cells in 1T1R cells



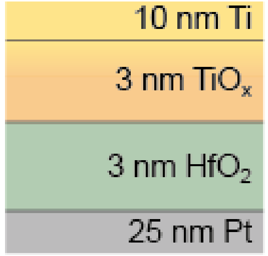
- One-transistor-one-resistor (1T1R) structures are the basic working elements of memristive arrays.
- Transitors act as selector and current compliance
- Transistors of different sizes exhibit varying transfer characteristics, which influence the electrical properties of memristor cells.


Stefan Wiefels

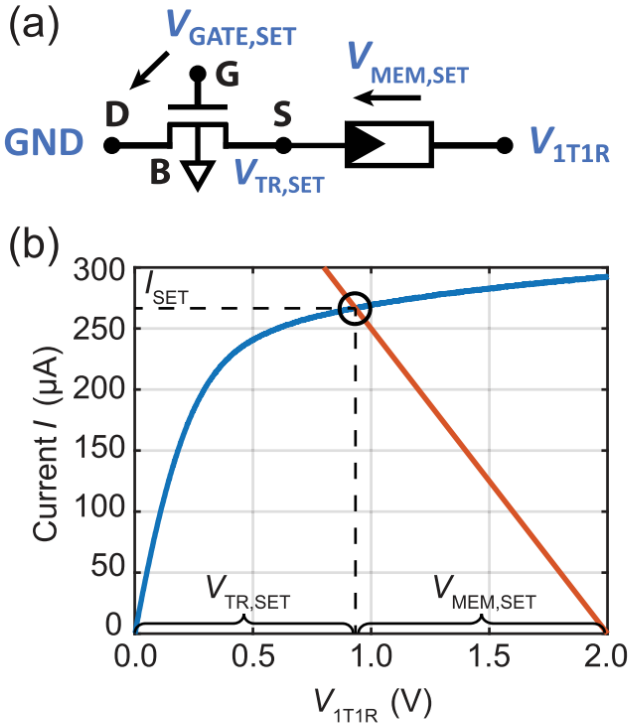

Xiaohua Liu

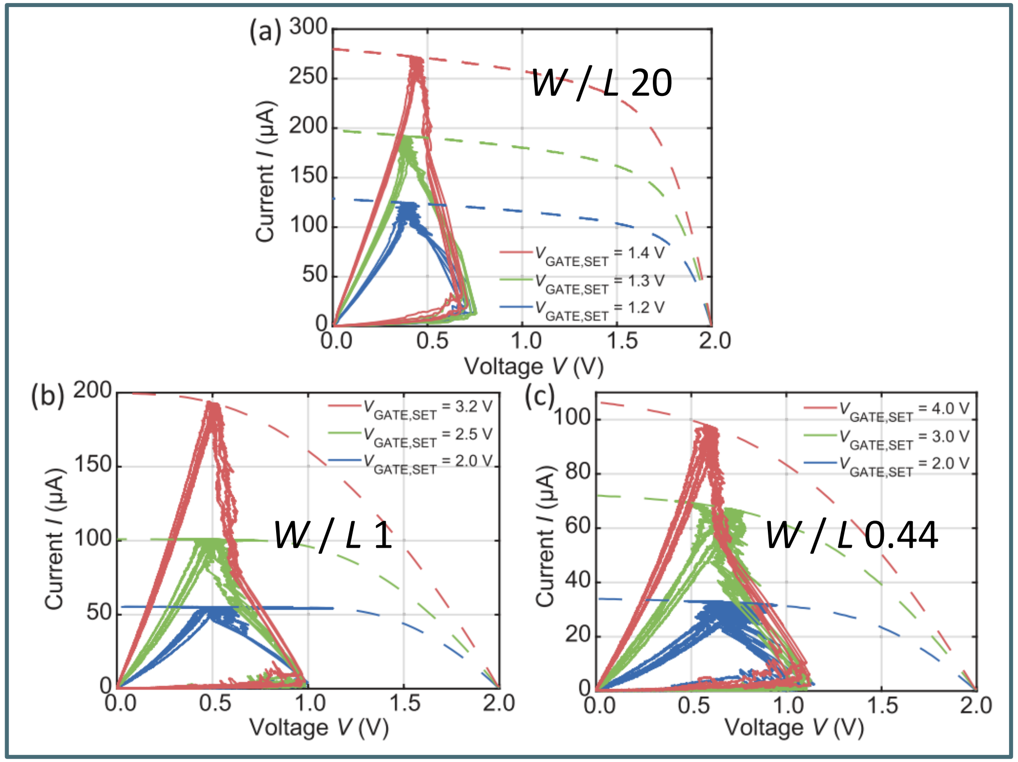
Intrinsic memristor voltage during SET process

Cüppers et al.
APL Mater. 2019



CMOS:
X-Fab 180nm

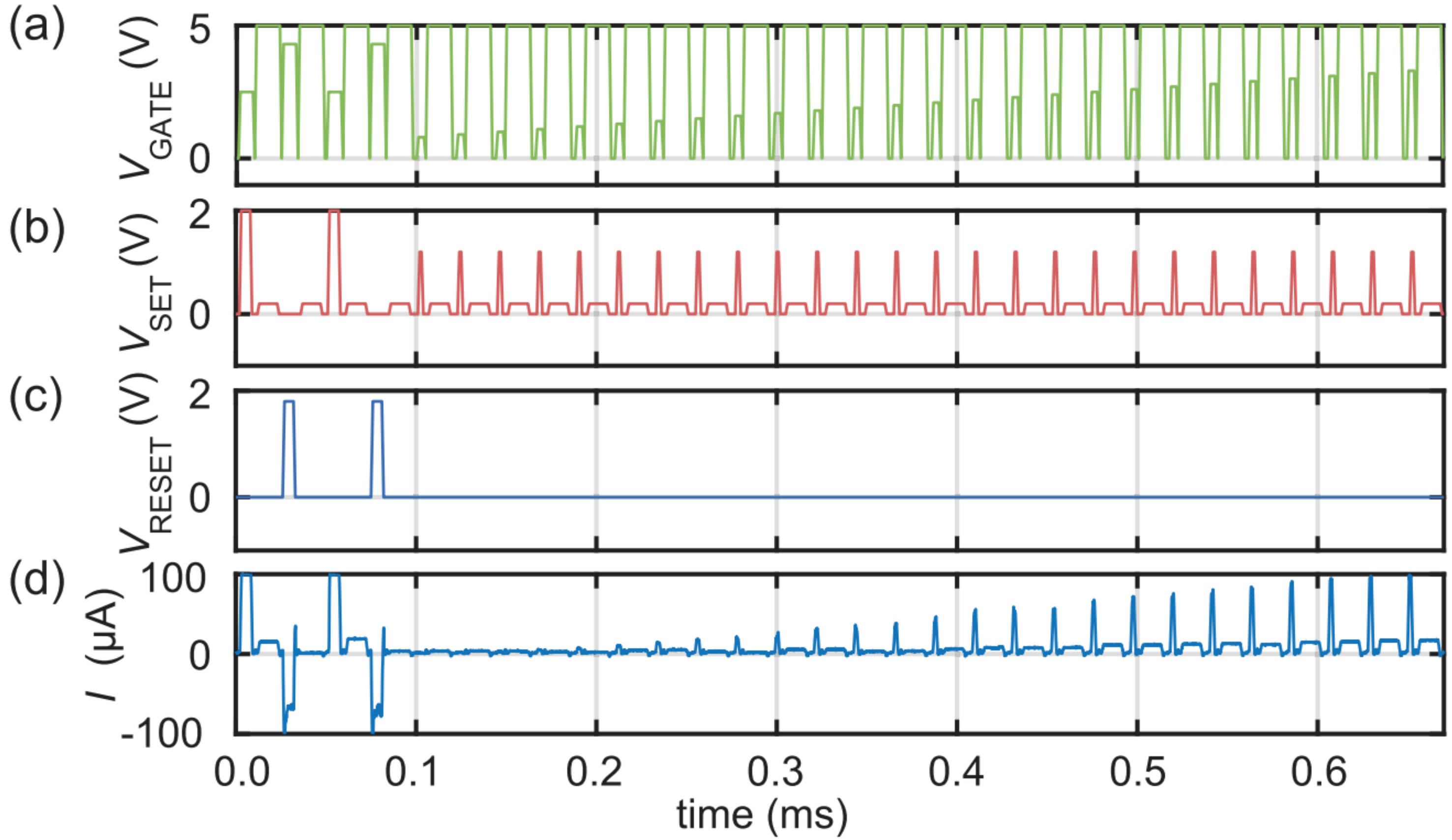




- Interplay of ReRAM cell and transistor analyzed using load line concept.
- Large-current transistors -> transistors work in saturation regime -> Transistors work as current compliance
- Small-current transistors -> From saturation regime to linear regime -> Transistors behave more like an ohmic resistor

Liu et al., IEEE TRANSACTIONS ON ELECTRON DEVICES (2024)

Incremental step pulse programming scheme for multilevel switching

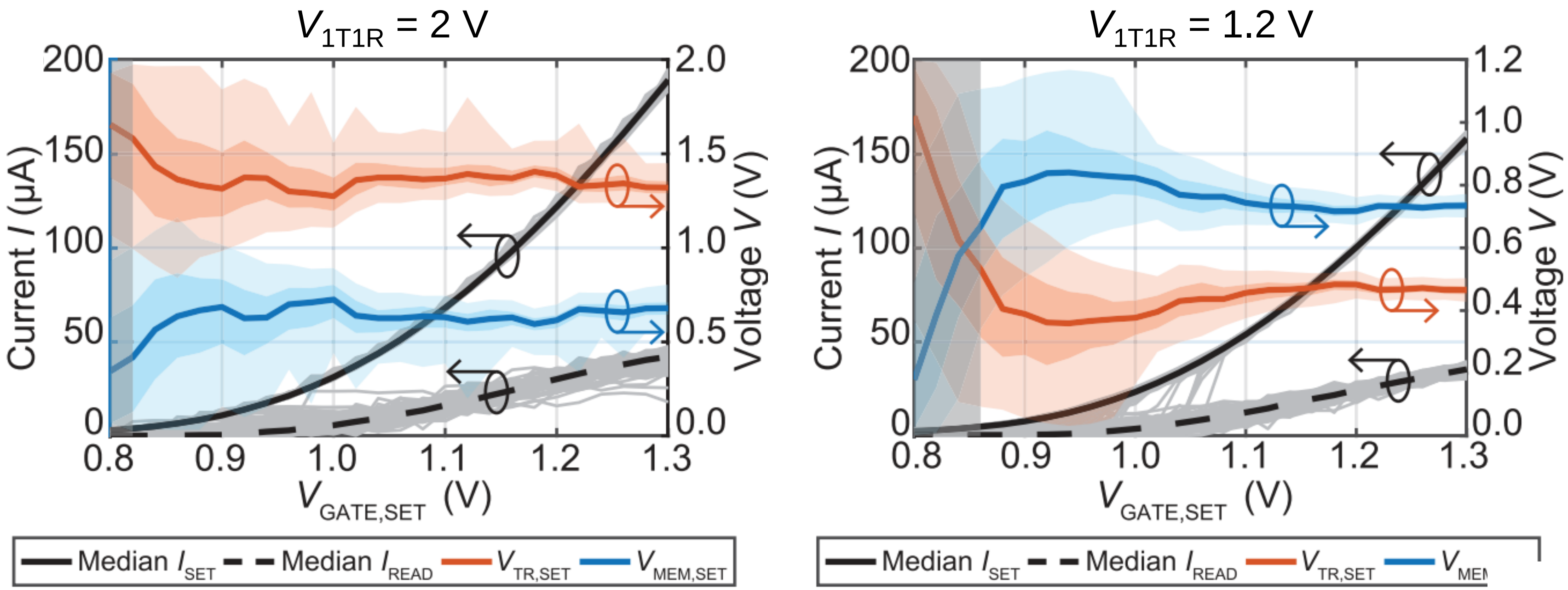


SET algorithm with program verify and incrementally increasing gate voltage applied to 1T1R samples

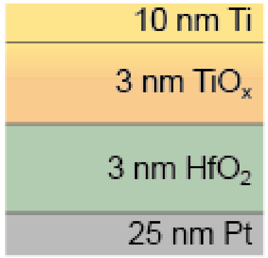
Liu et al., IEEE TRANSACTIONS ON ELECTRON DEVICES (2024)

Statistical results

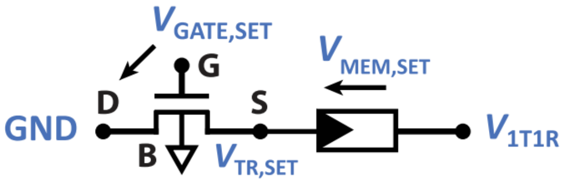
Evolution of the voltage division in 1T1R structure and correlation with transistor characteristics

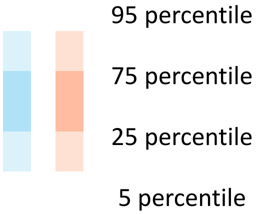


Cüppers et al.
APL Mater. 2019



CMOS:
X-Fab 180nm

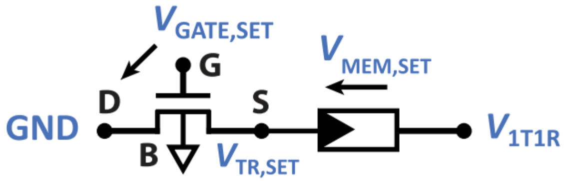


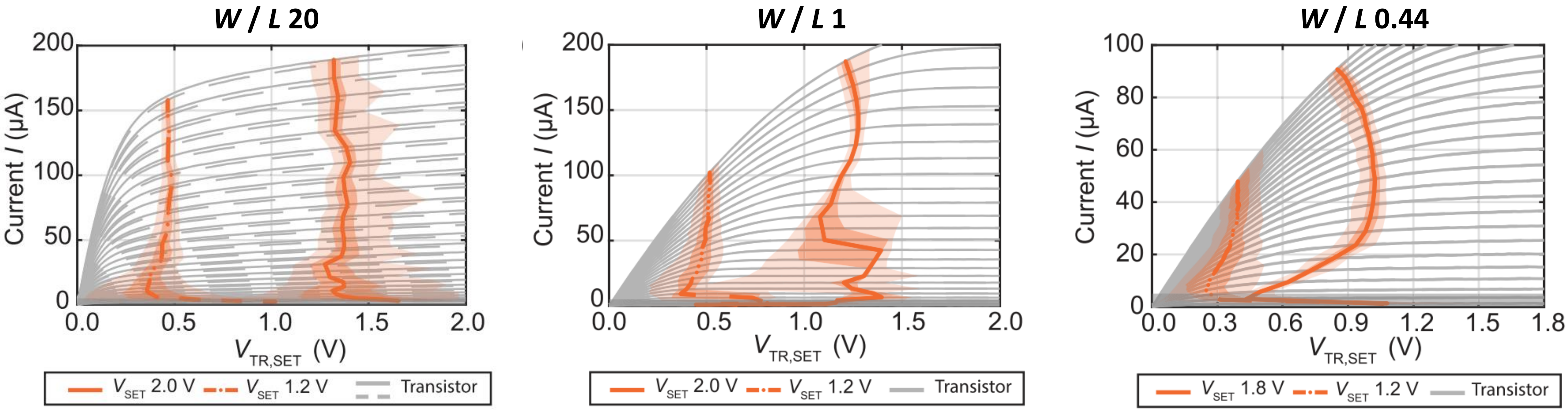


- The statistics of the 200-cycle SET algorithm test for 1T1R structures
- Voltage over ReRAM cell ($V_{MEM,SET}$) stays around 0.7 V.
- V_{1T1R} affects the voltage over the transistor ($V_{TR,SET}$). → High V_{1T1R} puts more stress to the transistor, but low V_{1T1R} might shift the switching characteristics to the voltage limited regime

Statistical results

Impact of transistor characteristic and biasing conditions on 1T1R structures





Decreasing transistor *W* / *L* ratio

95 percentile

75 percentile

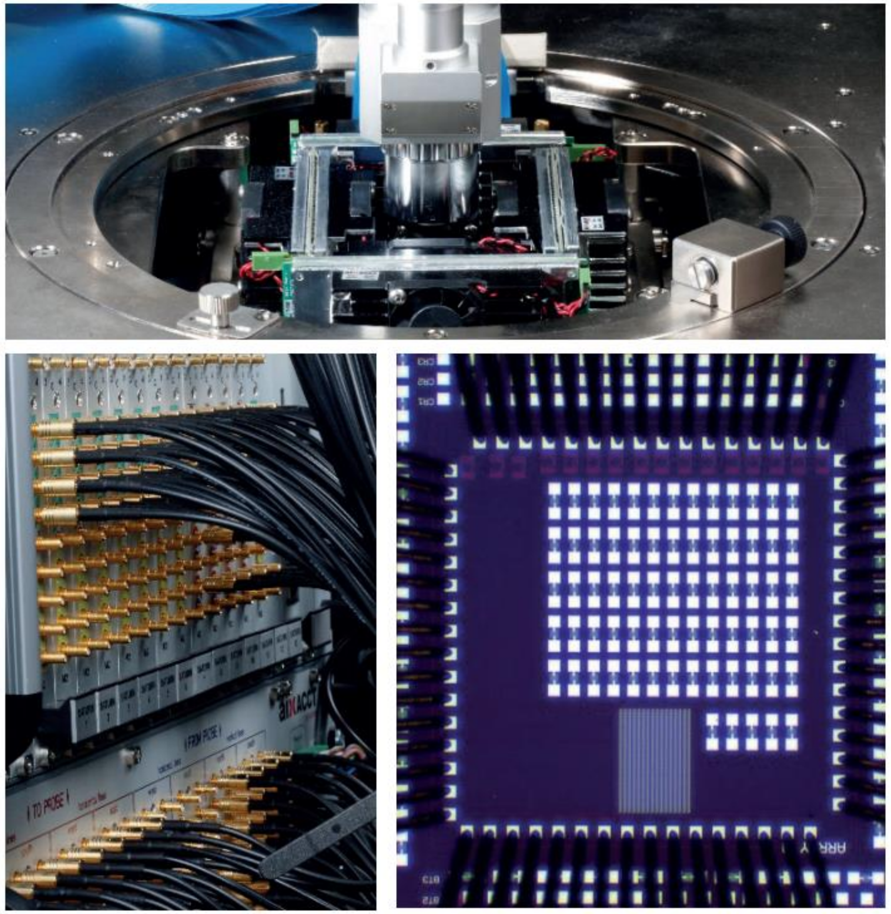
25 percentile

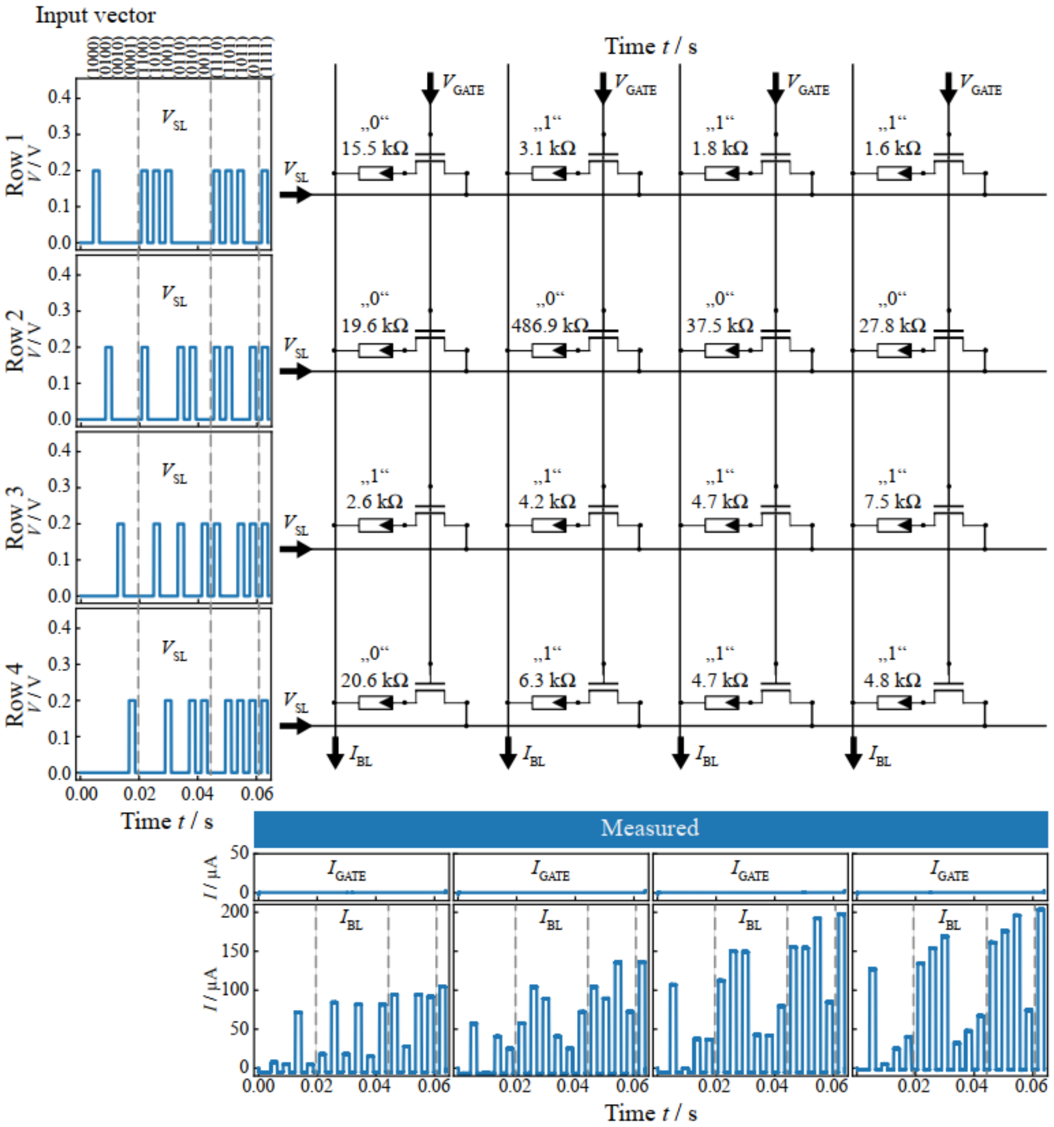
5 percentile

- Lower V_{1T1R} or lower *W*/*L* both shift the switching path away from the saturation regime, towards the ohmic / linear regime
  - ➢ More SET variability due to worse current control

Matrix array characterization

VMM demo on memristor array



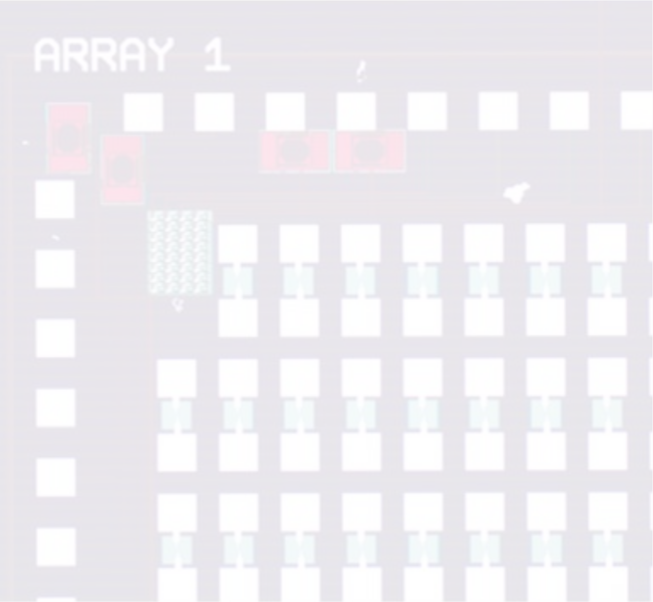


- 64 ch DAC: 200 MS/s, 16 bits → fast (100 ns) CC
- 32 ch ADC: 100 MS/s, 16 bits → I amp, 1 µA-10 mA

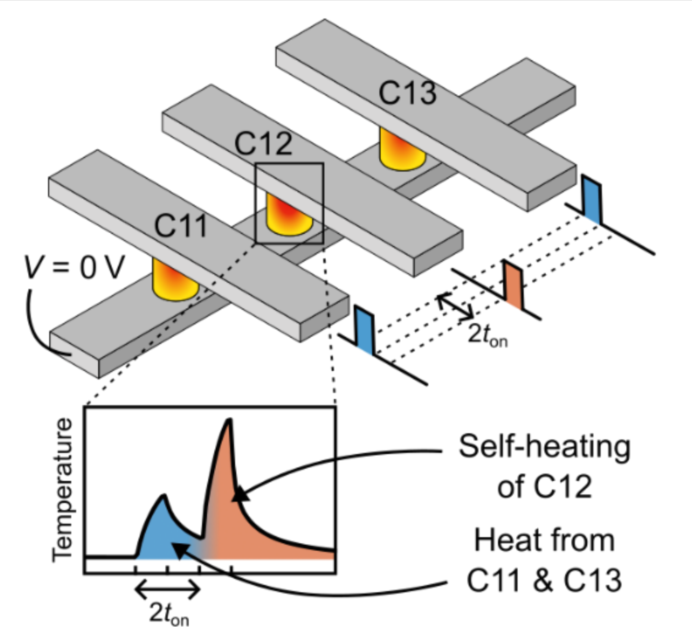
S. Wiefels et al., MetroXRAINE, IEEE, 2023.

Outline

1T1R memristor cross-bar arrays



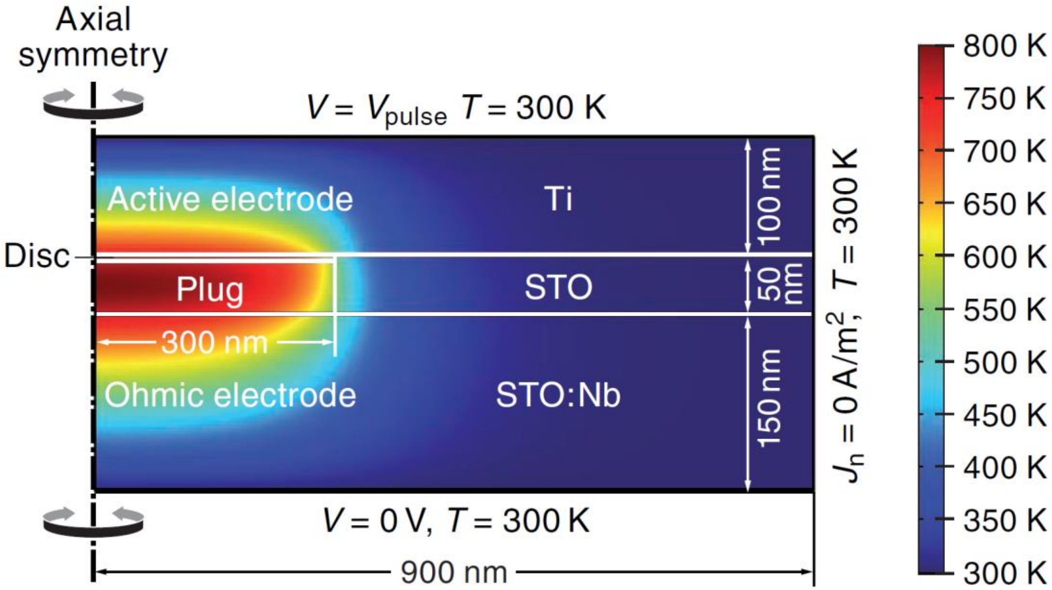
Spatio-temporal effects in cross-bar arrays

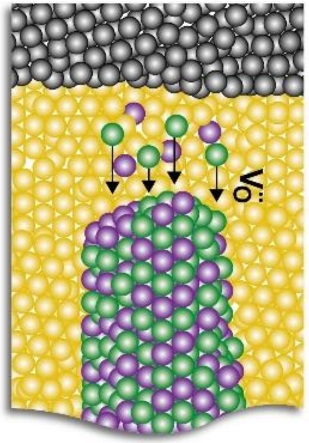


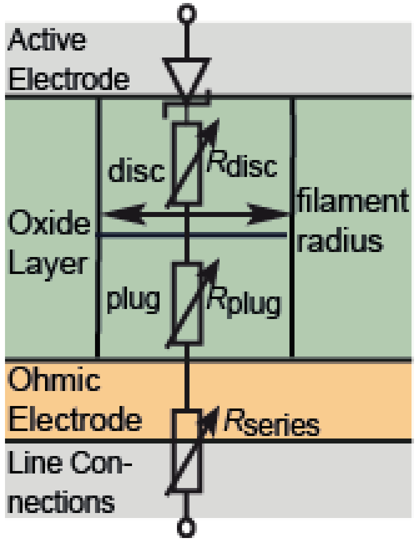
Valence change memory

Thermally accelerated ion drift and diffusion

Stephan Menzel





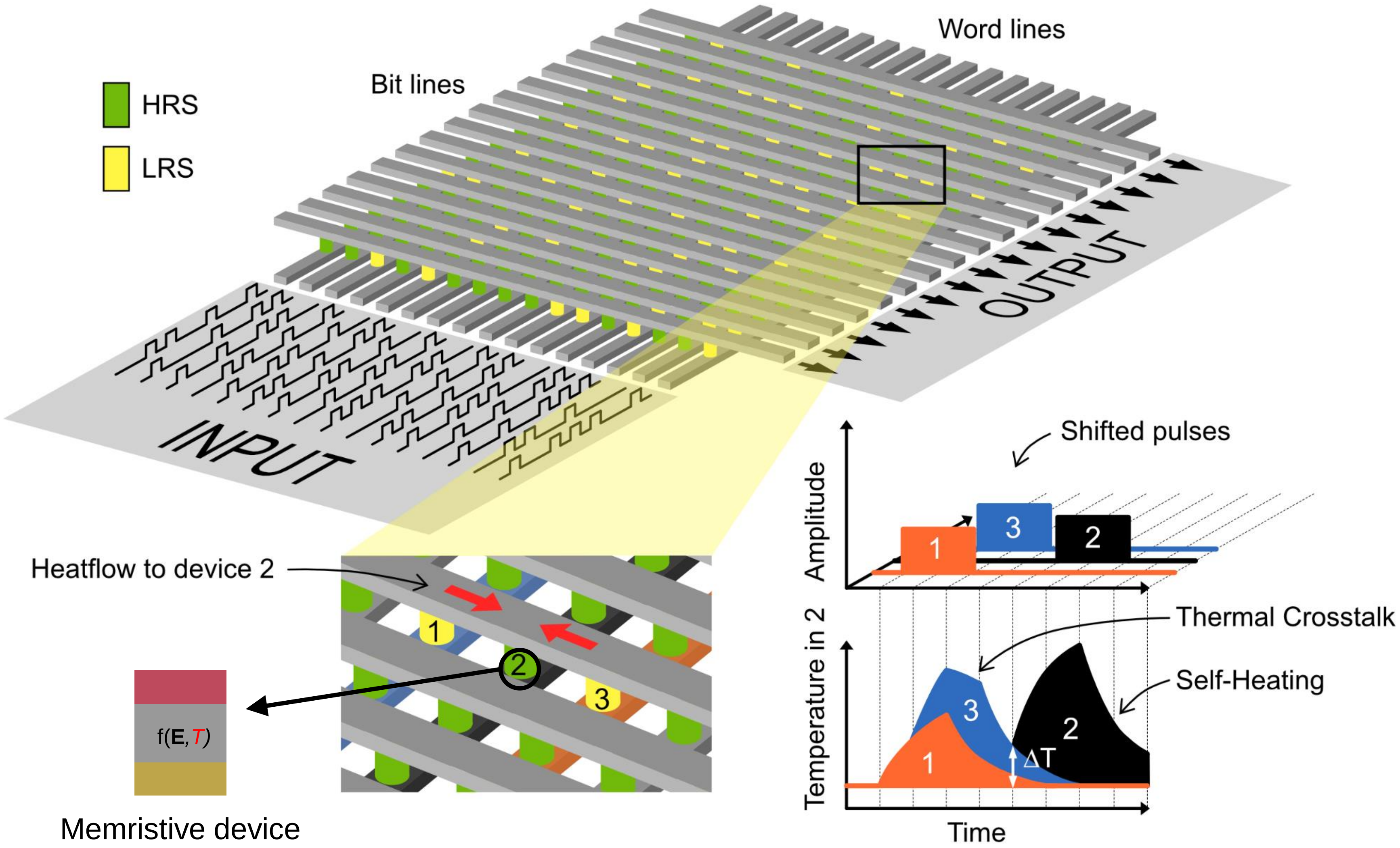


S. Menzel et al., Adv. Funct. Mater. (2011)

JART VCM v1b model

https://www.fz-juelich.de/en/pgi/pgi-7/research/research-groups-1/ag-menzel/jart-model

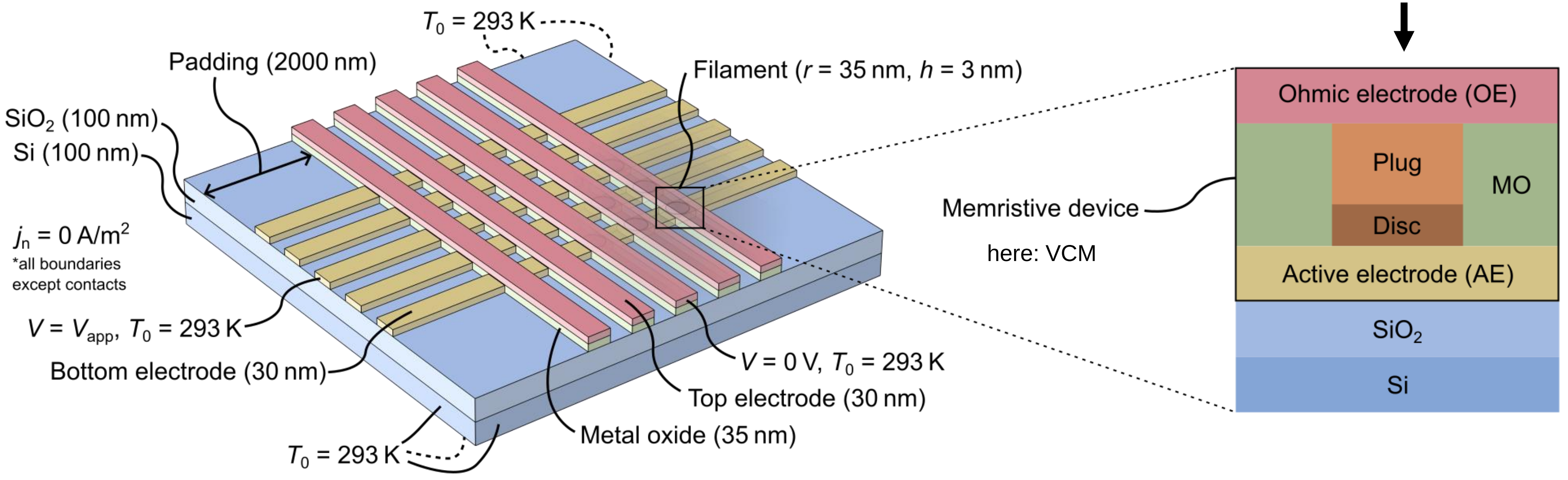
Memristive arrays for computing in memory



Daniel Schön

Crossbar array model

Could also be any other memristive device!



Electrothermal equations

Transient heat transfer equation

$$\rho_{\mathrm{m}} C_{\mathrm{p}} \frac{\partial T}{\partial t} - \nabla k \nabla T = \mathbf{j} \cdot \mathbf{E}$$

Current continuity equation

$$\nabla \cdot \mathbf{j} = -\nabla \sigma \nabla \phi = 0$$

Switching mechanism: JART VCM v1b

Variable electrical conductivity

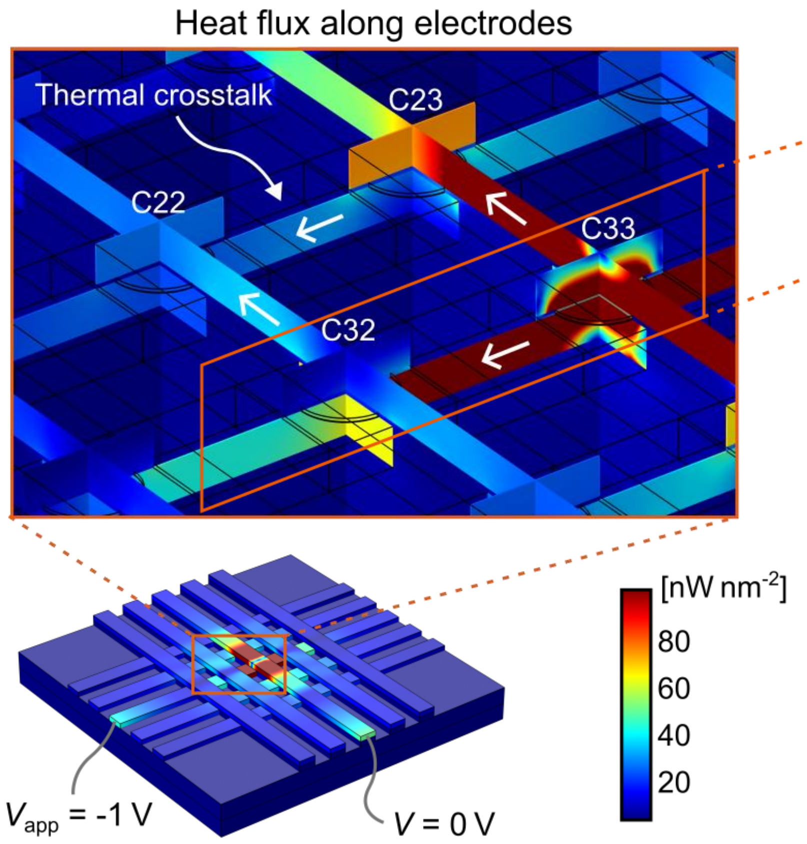
$$\sigma_{\mathrm{disc/plug}}(N_{\mathrm{disc/plug}}) = e z_{\mathrm{V_O}} N_{\mathrm{disc/plug}} \mu_{\mathrm{n}}$$

Oxygen vacancy concentration

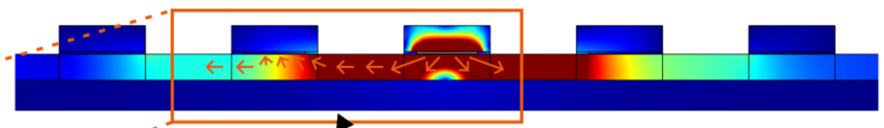
$$\frac{\mathrm{d}N_{\mathrm{disc}}}{\mathrm{d}t} = -\frac{I_{\mathrm{ion}}(N_{\mathrm{disc}}, V_{\mathrm{disc}}, T_{\mathrm{disc}})}{z_{\mathrm{V_O}} e A l_{\mathrm{disc}}}$$

Origin of thermal crosstalk

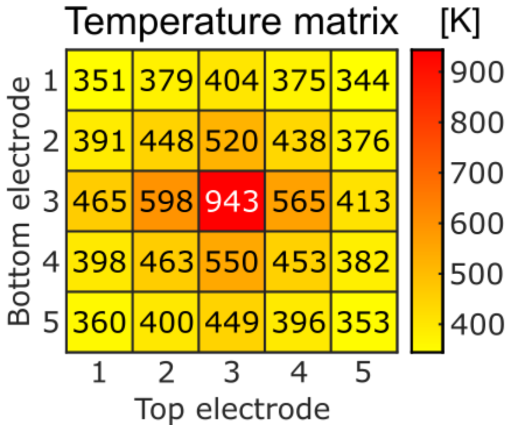
Heat flux along electrodes



Heat flux along selected bottom electrode

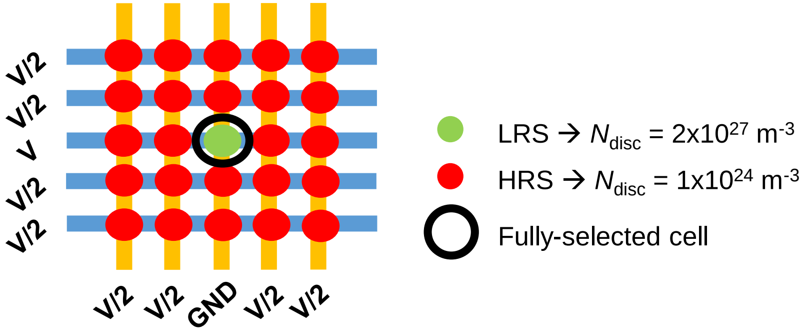


Heat is distributed via the electrode



Temperature matrix [K]

Bottom electrode \ Top electrode	1	2	3	4	5
1	351	379	404	375	344
2	391	448	520	438	376
3	465	598	943	565	413
4	398	463	550	453	382
5	360	400	449	396	353



- ● LRS → $N_{disc} = 2\text{x}10^{27}$ m^{-3}
- ● HRS → $N_{disc} = 1\text{x}10^{24}$ m^{-3}
- ○ Fully-selected cell

→ Heat transport via electrodes to adjacent devices

→ Additional heat contribution due to Joule heat of the line

Schön et al., Advanced functional materials 33 (22), 2213943 (2023)

Thermal crosstalk for different distances

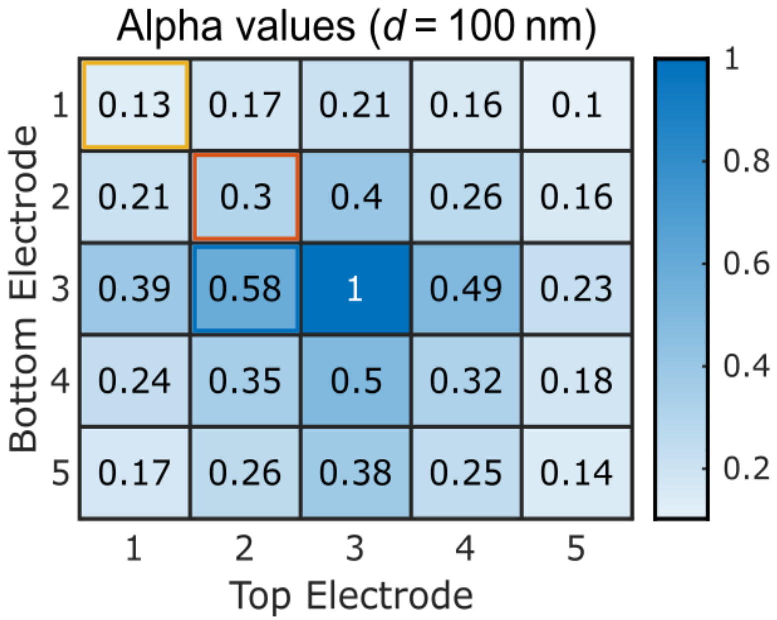
Thermal resistance

$$T_{\mathrm{sel}} = T_0 + R_{\mathrm{th}} P_{\mathrm{sel}}$$

Heat transfer coefficient

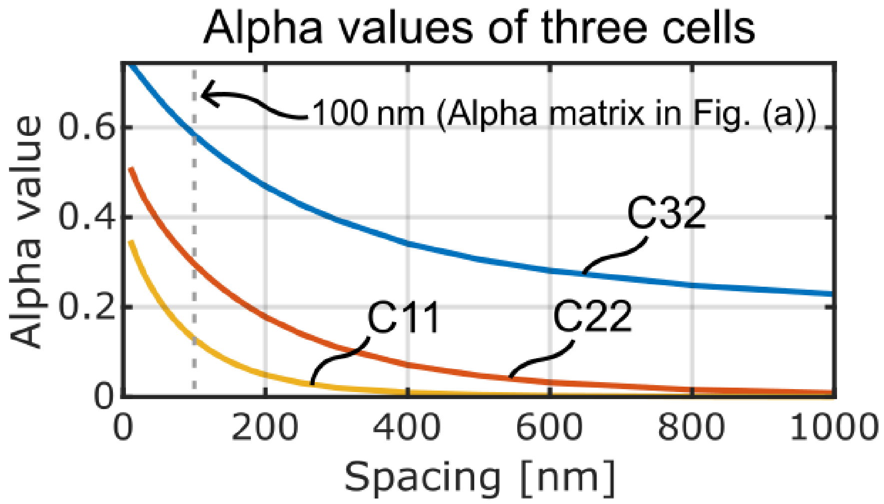
$$T_{\mathrm{ij}} = T_0 + \alpha_{\mathrm{ij}} R_{\mathrm{th}} P_{\mathrm{sel}}$$

$$\alpha_{\mathrm{ij}} = \frac{\Delta T_{\mathrm{ij}}}{\Delta T_{\mathrm{sel}}}$$



Alpha values (*d* = 100 nm)

Bottom Electrode \ Top Electrode	1	2	3	4	5
1	0.13	0.17	0.21	0.16	0.1
2	0.21	0.3	0.4	0.26	0.16
3	0.39	0.58	1	0.49	0.23
4	0.24	0.35	0.5	0.32	0.18
5	0.17	0.26	0.38	0.25	0.14

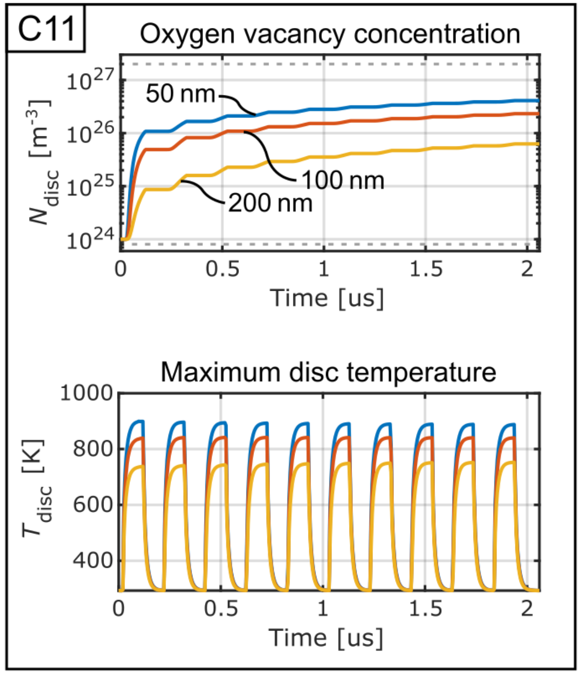


Alpha values of three cells

→ Joule heat of line is encoded in alpha value

→ Thermal crosstalk relevant for very spacings <100nm

Crosstalk in 1x3 line arrays



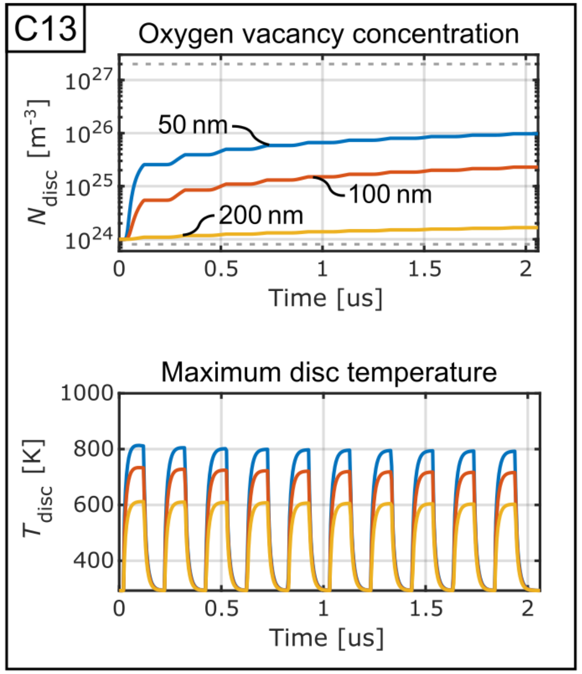
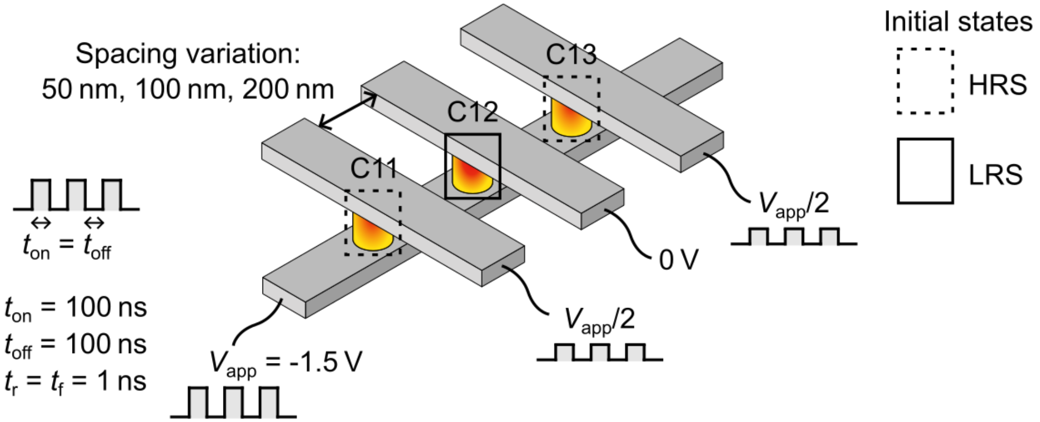


Illustration of thermal crosstalk simulation

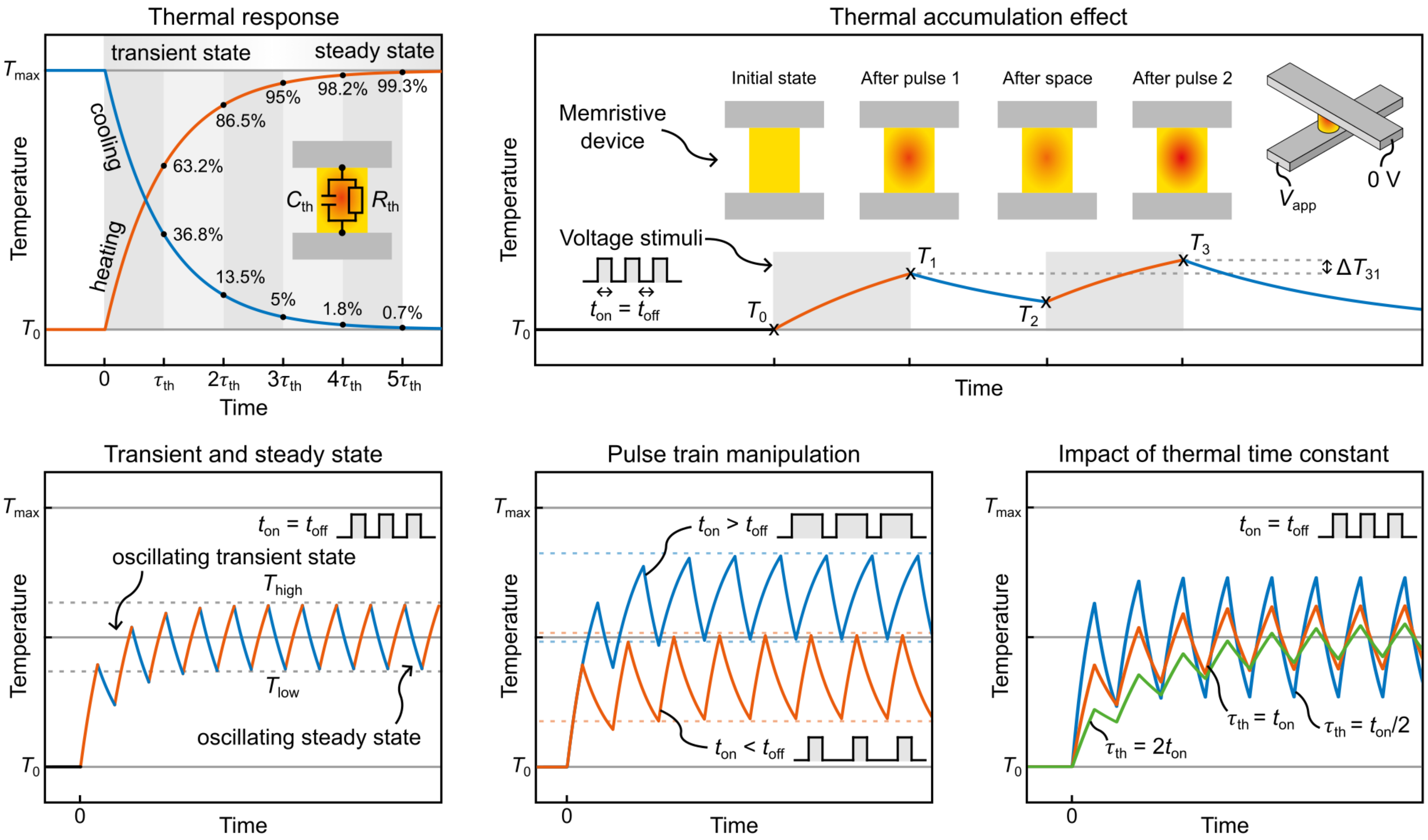


→ Gradual switching in adjacent cells

→ Synaptic potentiation in adjacent cells due to Thermal Crosstalk

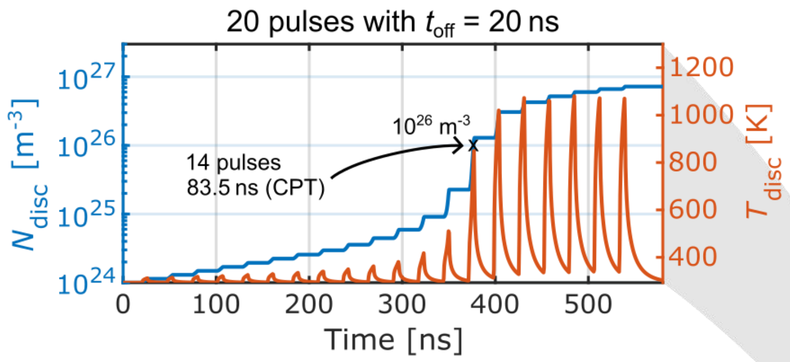
→ RESET operation: Process is reversed → depression

Thermal accumulation effect

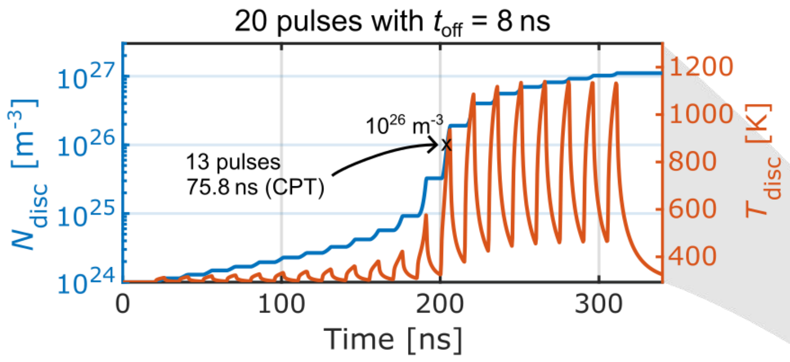


Schön et al., Advanced functional materials 33 (22), 2213943 (2023)

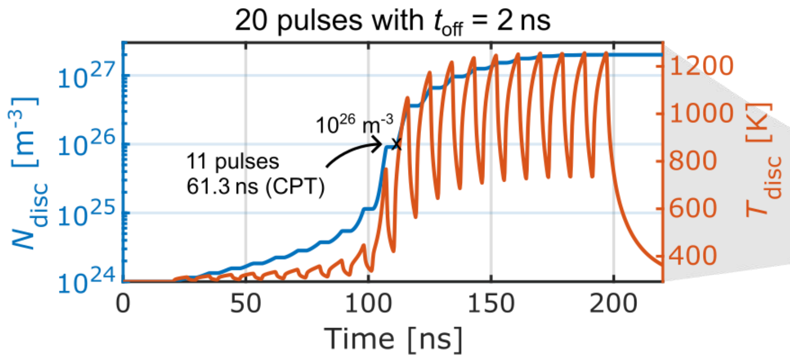
Thermal Accumulation Effect in one Cell: SET



20 pulses with t_{off} = 20 ns

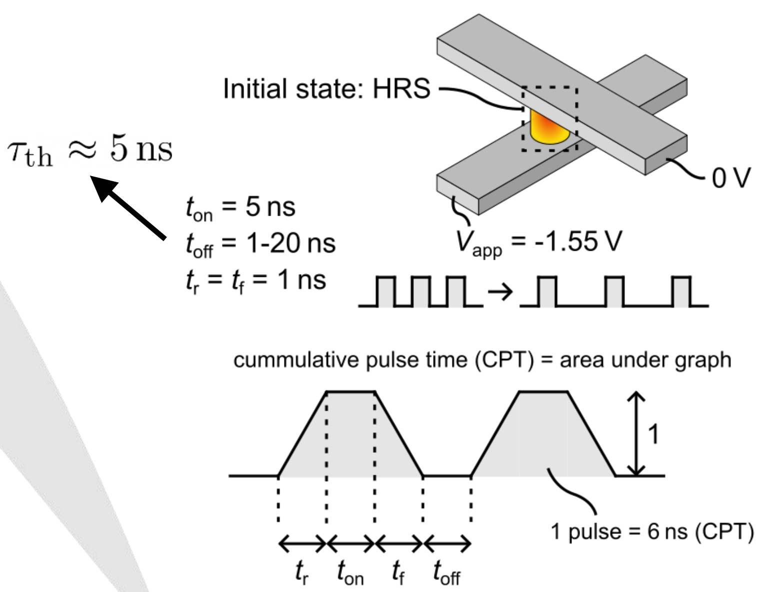


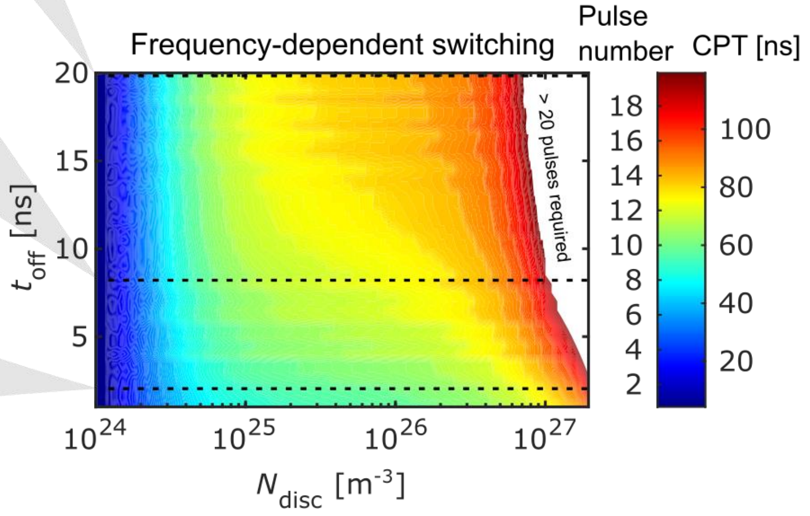
20 pulses with t_{off} = 8 ns



20 pulses with t_{off} = 2 ns

Illustration of thermal accumulation effect simulation

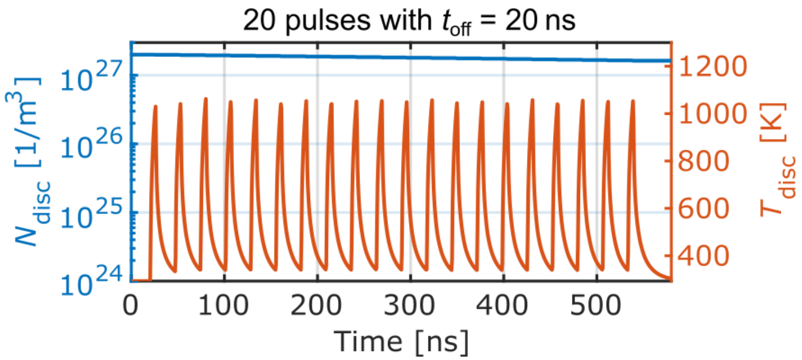


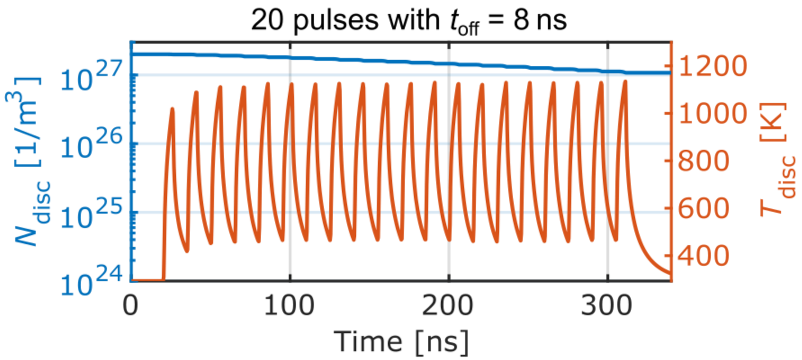


Frequency-dependent switching

→ Frequency-dependent switching time due to thermal accumulation

Thermal Accumulation Effect in one Cell: RESET


20 pulses with t_{off} = 20 ns


20 pulses with t_{off} = 8 ns

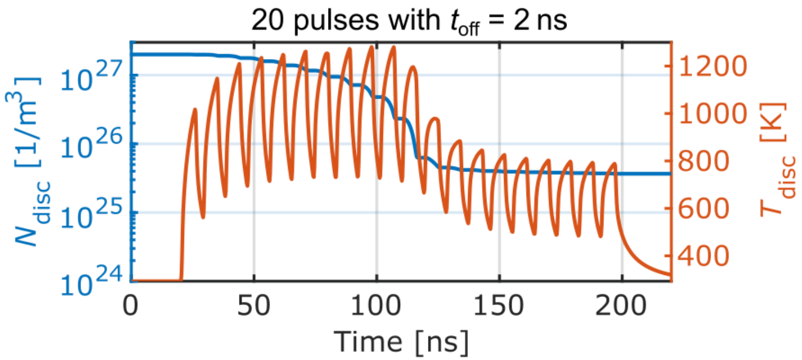
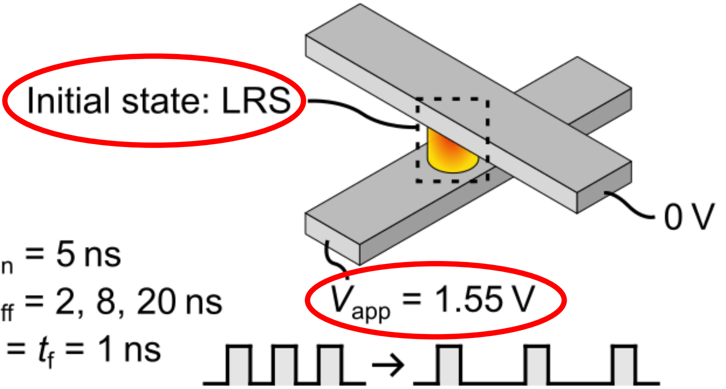

20 pulses with t_{off} = 2 ns

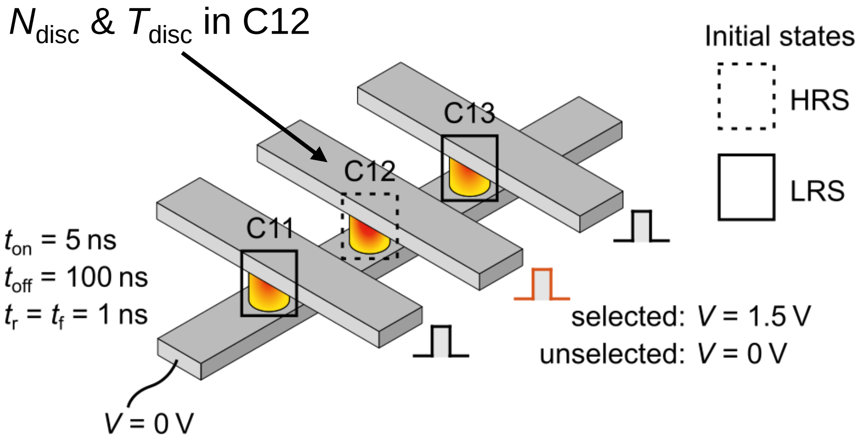
Illustration of thermal accumulation effect simulation



t_{on} = 5 ns
t_{off} = 2, 8, 20 ns
t_r = t_f = 1 ns

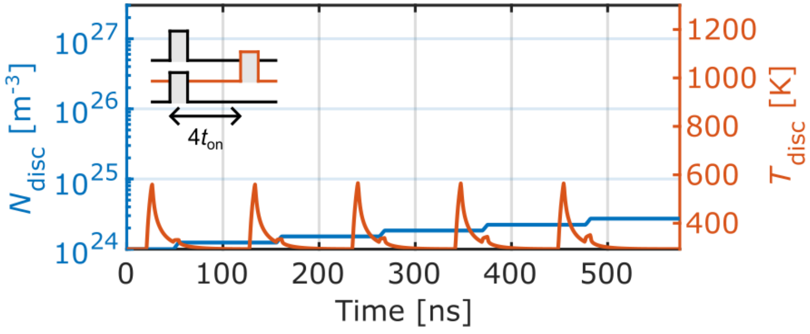
→ Frequency-dependent switching due to thermal accumulation effect

Spatio-Temporal Correlations in a 1x3 Line Array

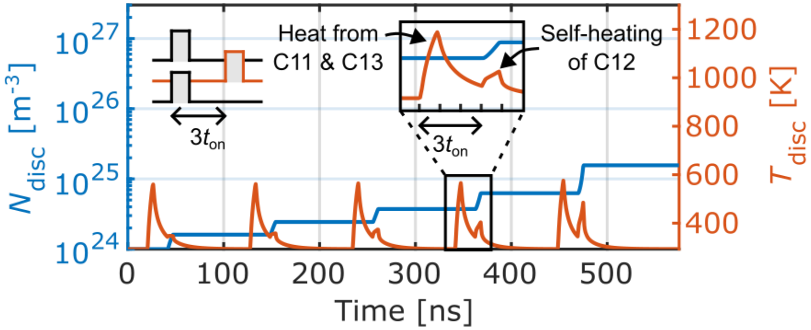


Schön et al., Adv. Function. Mater. 33 (22), 2213943 (2023)

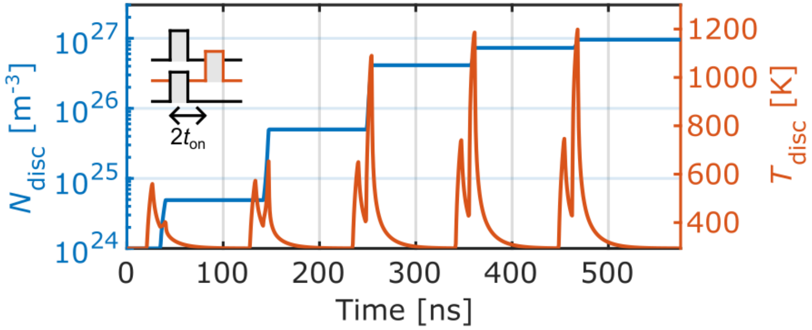
Evolution of N_{disc} and T_{disc} at long time offset



Evolution of N_{disc} and T_{disc} at medium time offset



Evolution of N_{disc} and T_{disc} at short time offset

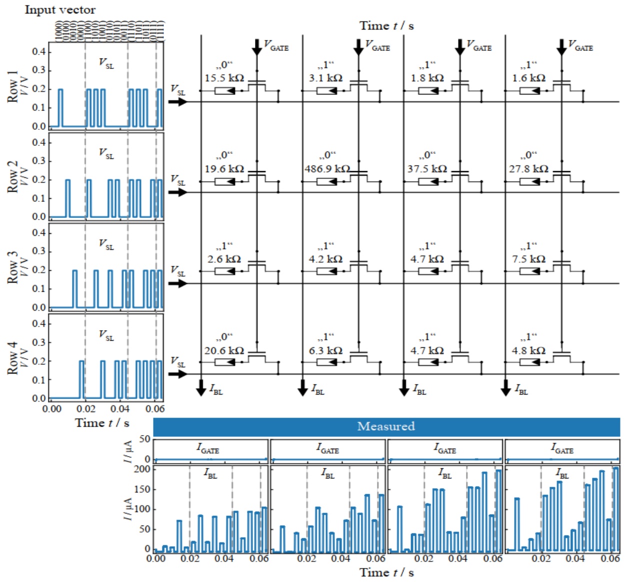


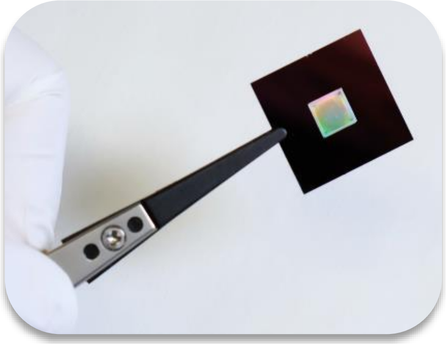
→ *T* as second state variable is transferred to surrounding cells

Summary

1T1R elements in memristor crossbar arrays

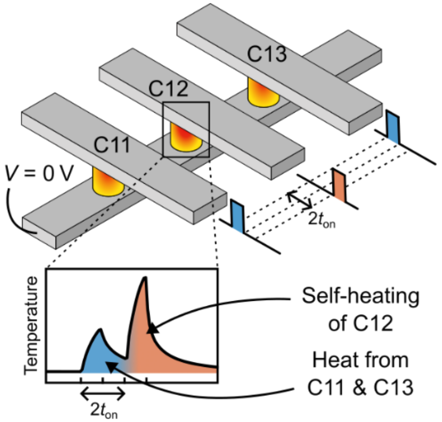
- ✓ Successful CMOS integration of memristors on 180nm X-Fab and 28nm TSCM
- ✓ Interplay between memristor and transistor ⇒ design rules for 1T1R blocks
- ✓ Programming algorithm for analog programming ⇒ demonstration of VM multiplication





Spatio-temporal effects in memristor arrays

- ✓ Thermal correlation effects (crosstalk) occur **below 100-200 nm** due to heat transport along metal electrodes
- ✓ **Thermal accumulation** effects if pulse length and delays are below the thermal time constant
- ✓ **Spatial-temporal thermal effects** occur for small distances and delays below the thermal time constant ⇒ learning in memristor networks



Great thanks to the team @ PGI-7

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