Integrating programmable plasticity in experiment descriptions for analog neuromorphic hardware

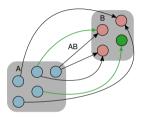
Philipp Spilger^{1,2,*}, Eric Müller¹, Johannes Schemmel² 2025-03-25

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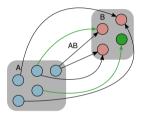


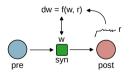
Programmable plasticity



• **plasticity**: altering topology or parameterization during experiment runtime according to decisions made on real time observations

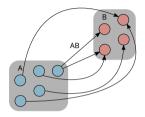
Programmable plasticity





- **plasticity**: altering topology or parameterization during experiment runtime according to decisions made on real time observations
- **programmable**: "freely"-configurable algorithm and execution schedule

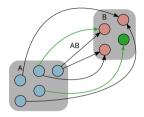
Using mixed-signal neuromorphic hardware



- topology description
 - populations of neurons, projections of synapses

• pre-defined experiment protocol

Using mixed-signal neuromorphic hardware

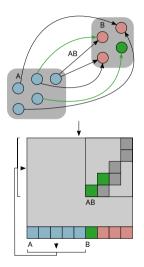


- topology description
 - populations of neurons, projections of synapses

+ plasticity

• pre-defined experiment protocol

Using mixed-signal neuromorphic hardware



- topology description
 - populations of neurons, projections of synapses
 - + plasticity
 - unplaced!
- pre-defined experiment protocol
- automated translation/mapping to/from hardware
 - placement
 - calibration
 - routing
 - data transform

- developed in Heidelberg
- \bullet analog AdEx neurons and COBA/CUBA synapses
- 1000 × network dynamic speed-up



HW: Pehle et al.



SW: Müller et al.



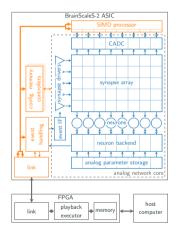
- 512 neurons with 256 synapses each
- two embedded SIMD plasticity processors
- layered software, multiple front ends



HW: Pehle et al.



SW: Müller et al.



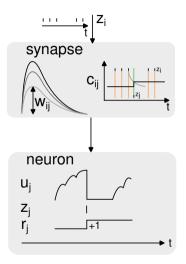
Plasticity on BrainScaleS-2: Embedded processor observables

controllables:

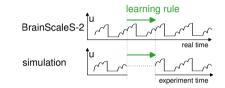
- synaptic weight (6 bit)
- neuron parameterization
- . . .

observables:

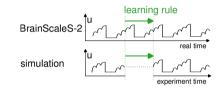
- parallel ADC recording (8 bit)
 - synaptic correlation (causal, acausal)
 - neuron membrane/adaptation/synaptic inputs
- firing rate per neuron (spike counter, 1+8 bit)

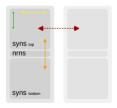


 learning rule execution duration limited: concurrent time-continuous evolution of network dynamics

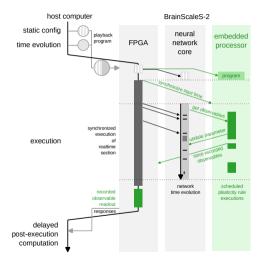


- learning rule execution duration limited: concurrent time-continuous evolution of network dynamics
- physical locality
- available memory
- calculation accuracy (no hardware float)

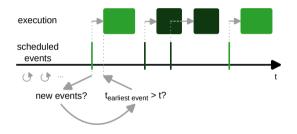




Plasticity abstraction: execution model



- JIT-compiled program for embedded processors
- synchronized execution of neural network evolution and timed plasticity on processors
- scheduling of potentially multiple (sequential or alternating) plasticity rules



earliest-deadline-first scheduler

- fixed latency from passed deadline to rule execution
- low computational overhead
- supports dynamic rule execution schedule

Plasticity abstraction: user interface in PyNN

import pynn_brainscales.brainscales2 as pynn

```
class MyPlasticity(pynn.PlasticityRule):
    def __init__(self, timing, recording):
        ...
    def generate_kernel(self) -> str:
        return "... embedded processor code ..."
my_plasticity = MyPlasticity(...)
pop = pynn.Population(
        ...,
    Neuron(plasticity_rule=my_plasticity))
proj = pynn.Projection(
        ....,
```

```
Synapse(plasticity_rule=my_plasticity))
```

```
# ... experiment protocol
```

```
proj.get_data("my_syn_obsv")
pop.get_data("my_nrn_obsv")
```

- plasticity rule
 - timing
 - recording
 - code for the embedded processor
- acting on network elements
- post-execution access to recorded data

```
void PLASTICITY_RULE_KERNEL(
    array<SynapseArrayViewHandle, N> const& synapses,
    array<NeuronViewHandle, M> const& neurons)
{ ... }
```

- embedded processor code
 - functional interface
 - access to network entities

- code generation for
 - rule scheduling
 - network entity handles

Plasticity abstraction: kernel code & data flow

```
void PLASTICITY_RULE_KERNEL(
    array<SynapseArrayViewHandle, N> const& synapses,
    array<NeuronViewHandle, M> const& neurons,
    Recording& recording)
{ ... }
```

```
observables = {
```

```
"my_obsv": PlasticityRule.ObservablePerSynapse(
    uint8, LayoutPerRow.packed),
```

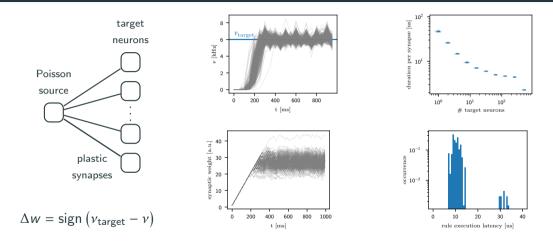
```
}
```

```
struct Recording
```

```
{
   ObsvPerSynPacked<uint8_t> my_obsv;
   ...
};
```

- embedded processor code
 - functional interface
 - access to network entities
 - access to recording
- customizable observable specification
- code generation for
 - rule scheduling
 - network entity handles
 - recording structure

Evaluation via simple homeostatic rule



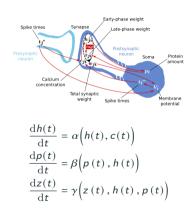
Application Dietrich et al. Sequence Learning with Analog Neuromorphic Multi-Compartment Neurons and On-Chip Structural STDP, ACAIN 2024. Application Atoui et al. Multi-timescale synaptic plasticity on analog neuromorphic hardware, NICE 2025.

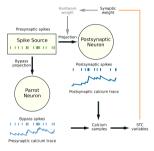
Poster: Atoui et al. Multi-timescale synaptic plasticity on analog NMHW

Plasticity in biology

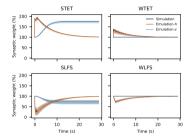
Plasticity on BrainScaleS-2

Results



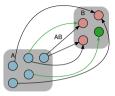


- Adaptation traces for emulating calcium
- Reduced precision (integer arithmetics)



 Accurate emulation of the plasticity rule





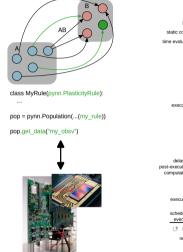
class MyRule(pynn.PlasticityRule):

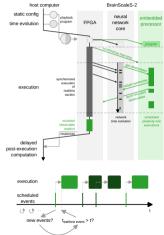
pop = pynn.Population(...(my_rule))

pop.get_data("my_obsv")

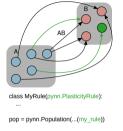


Summary



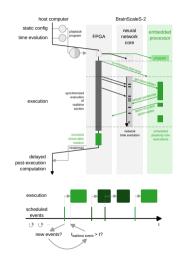


Summary

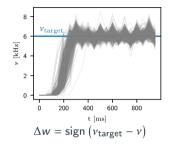


pop.get_data("my_obsv")

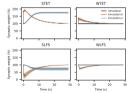








Poster Multi-timescale synaptic plasticity



Outlook

- embedded processor hardware optimizations
 - SIMD unit instruction set enhancements (floats?)
- domain-specific language for plasticity rule code
 - removes need for low-level knowledge about the embedded processors
- combining online plasticity and gradient-based learning
 - meta-learning on plasticity rule hyperparameters, local regularization

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