The Neuromorphic Computing Platform

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HBP & Dutch Neuroscience: Shaping Collaborations

Human Brain Project

Co-funded by
the European Union

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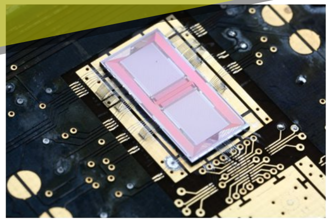
Why focus on the brain ? Three Reasons

- **Understanding the brain (Unifying Science Goal)**
  - Underpins what we are,
  - Data & knowledge are fragmented,
  - Integration is needed,
  - Large scale collaborative approach is essential.
- **Understanding brain diseases (Society)**
  - Costs Europe over €800 Billon/year,
  - Affects 1/3 people,
  - Number one cause of loss of economic productivity,
  - No fundamental treatments exist or are in sight
  - Pharma companies pulling out of the challenge.
- **Developing Future Computing (Technology)**
  - Computing underpins modern economies,
  - Traditional computing faces growing hardware, software, & energy barriers,
  - Brain can be the source of energy efficient, robust, self-adapting & compact computing technologies,
  - Knowledge driven process to derive these technologies is missing.



Neuromorphic Computing

Subproject 9 of the HBP

Subproject Leader: Steve Furber

Deputy Leader: Johannes Schemmel

- Neuromorphic Machines
- Algorithms and Architectures for Neuromorphic Computing
  - Theory
  - Applications

Co-funded by the European Union

The HBP Neuromorphic Computing Strategy

Next generation of NMC is more biology driven

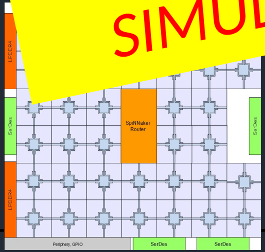
1st generation SpiNNaker-1 Machine

y-core system
on ARM cores
me simulator

Many-core Architecture

SIMULATION

Towards 2n



152 Cortex M4F per chip
36 GIPS/Watt per chip
x10 with constant power

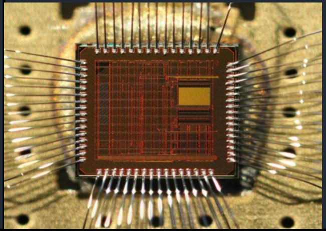
1st generation BrainScaleS-1 Machine

Physical model system
4M neurons, 1B plastic syn.
ccelerated emulator

Physical mode

EMULATION

Towards 2nd



On-chip plasticity processors
Flexible hybrid plasticity
Active dendrites

Designed and built from the transistor up !

Neuromorphic systems worldwide

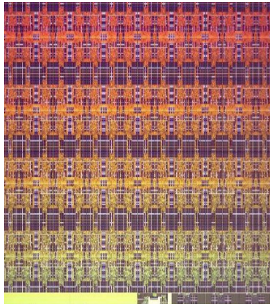
– state-of-the-art and complementarity

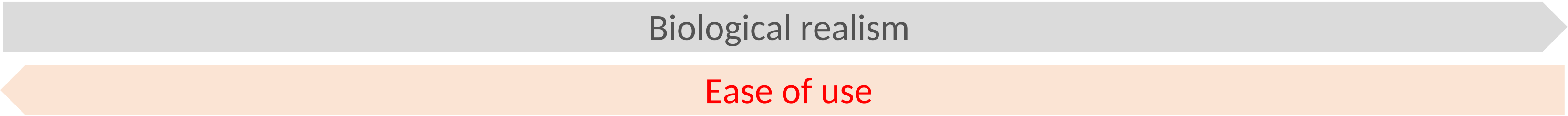
SpiNNaker
Biologically Inspired Massively Parallel Architectures

IBM
TrueNorth

intel
Loihi

BrainScaleS





Biological realism

Ease of use

Many-core (ARM) architecture Optimized spike communication network Programmable local learning x0.01 real-time to x10 real-time	Full-custom-digital neural circuits No local learning (TrueNorth) Programmable local learning (Loihi) Exploit economy of scale x0.01 real-time to x100 real-time	Analog neural cores Digital spike communication Biological local learning Programmable local learning x10.000 to x1000 real-time

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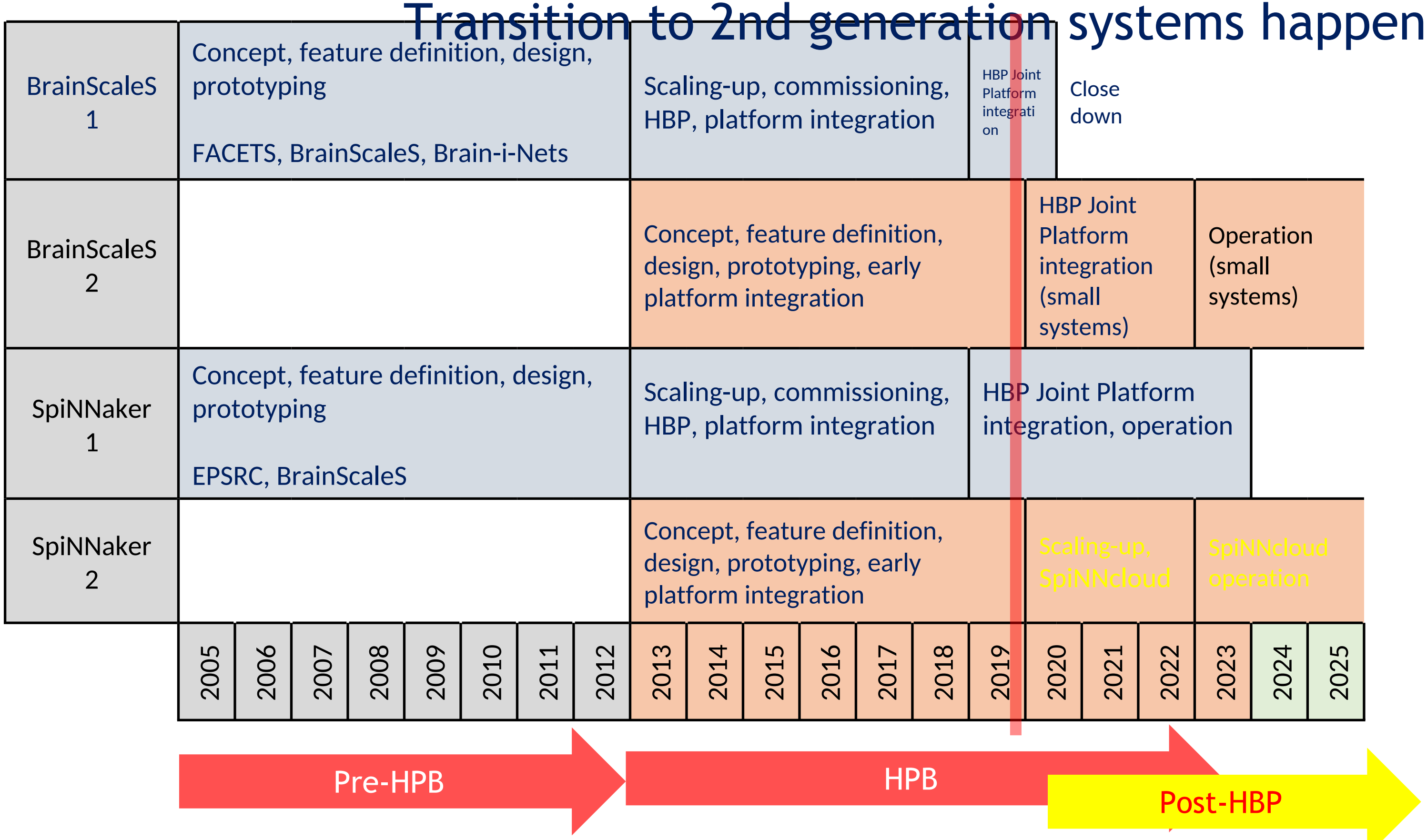
20 year NMC roadmap 2005-2025 (from pre- to post-HBP)

Transition to 2nd generation systems happens now



BrainScaleS 1	Concept, feature definition, design, prototyping FACETS, BrainScaleS, Brain-i-Nets	Scaling-up, commissioning, HBP, platform integration	HBP Joint Platform integration	Close down	
BrainScaleS 2		Concept, feature definition, design, prototyping, early platform integration		HBP Joint Platform integration (small systems)	Operation (small systems)
SpiNNaker 1	Concept, feature definition, design, prototyping EPSRC, BrainScaleS	Scaling-up, commissioning, HBP, platform integration	HBP Joint Platform integration, operation		
SpiNNaker 2		Concept, feature definition, design, prototyping, early platform integration		Scaling-up, SpiNNcloud	SpiNNcloud operation
	2005 2006 2007 2008 2009 2010 2011 2012	2013 2014 2015 2016 2017 2018	2019	2020 2021 2022	2023 2024 2025

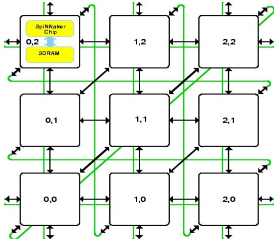
Pre-HPB

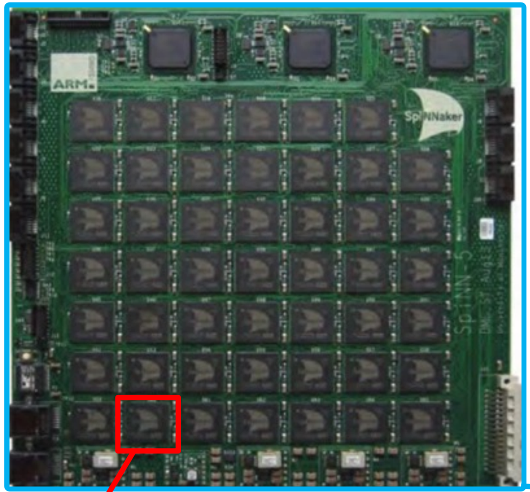
HPB

Post-HBP

SpiNNaker machines

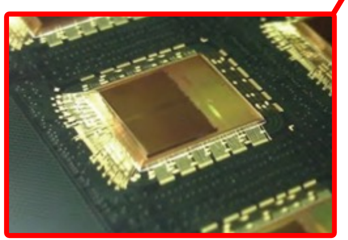
SpiNNaker board
(864 ARM cores)





- HBP platform
  - 1M cores
  - 11 cabinets (including server)
- Launch 30 March 2016
  - then 500k cores
  - 116 remote users
  - 6,530 SpiNNaker jobs run

SpiNNaker chip
(18 ARM cores)



SpiNNaker racks
(1M ARM cores)

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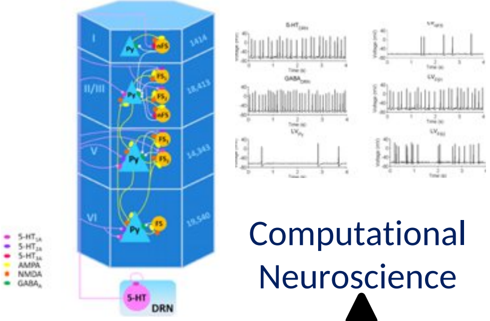
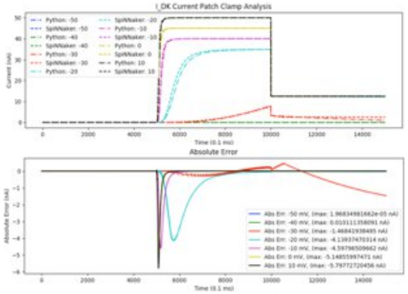
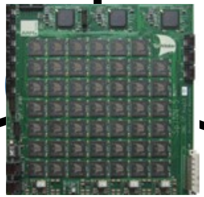
SpiNNaker applications

SpiNNaker
Biologically Inspired Massively Parallel Architectures



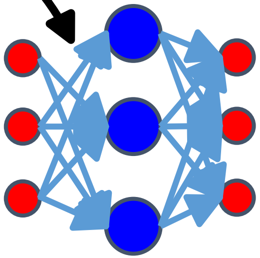


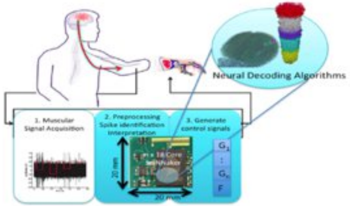
Computational Neuroscience

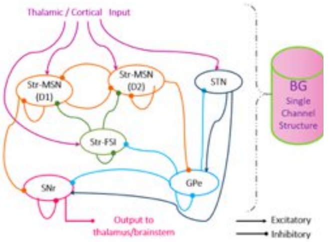


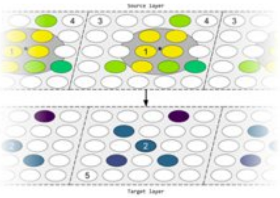
Neurorobotics

Theoretical Neuroscience

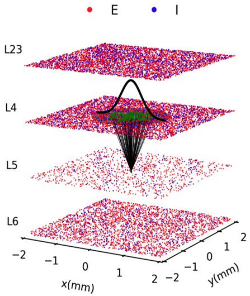


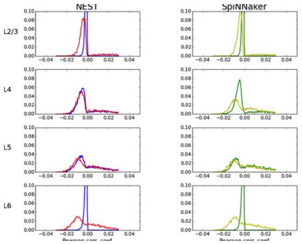




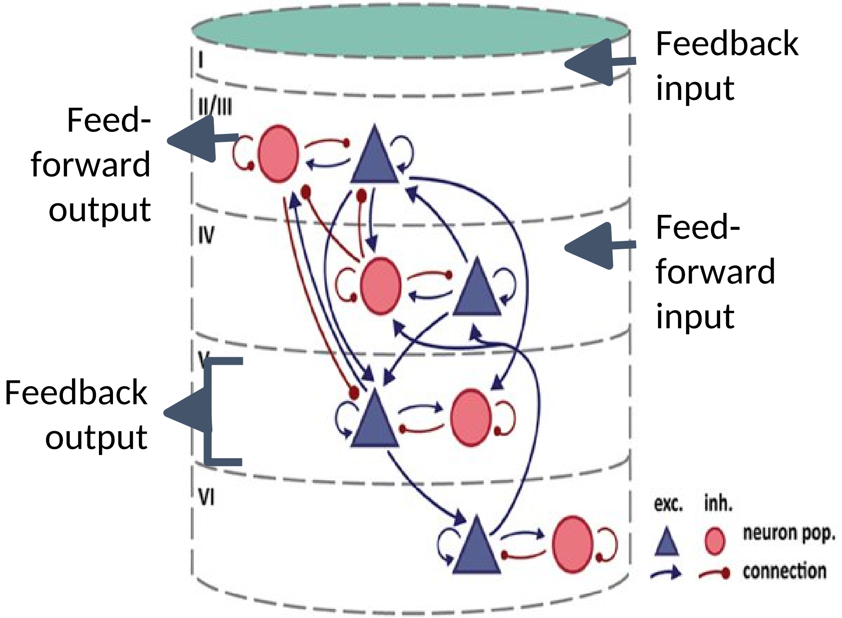


Cortical microcircuit





- ***Realtime execution of cortical model***
  - 1mm^2 cortex
    - 77k neurons
    - 285M synapses
    - 0.1 ms time-step
- ***Best previous versions of this model***
  - HPC: 3x slow-down
  - GPU: 2x slow-down
- ***Will scale to 100mm^2 without slow-down***
  - on current machine, simply by using more boards



Feedback input

Feed-forward output

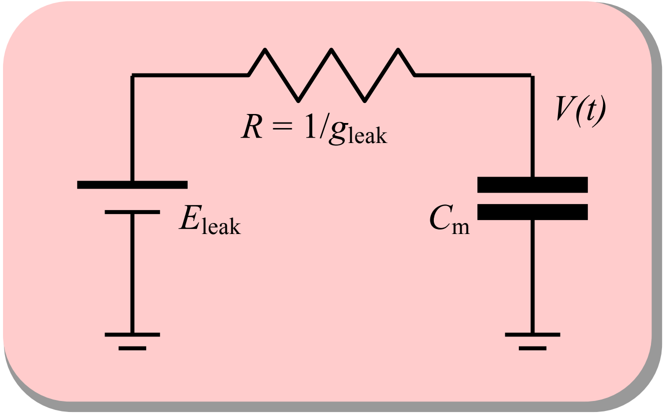
Feed-forward input

Feedback output

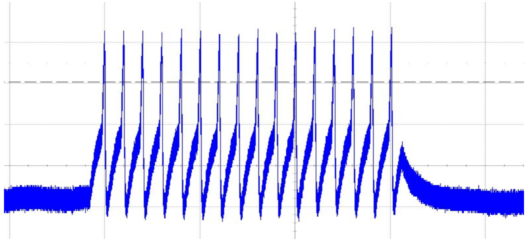
Oliver Rhodes, Luca Peres, Andrew G. Rowley, Andrew Gait, Luis A. Plana, Christian Brenninkmeijer & Steve.B. Furber, "*Real-time cortical simulation on neuromorphic hardware*", Phil Trans Roy Soc A, December 2019.

BrainScaleS: neuromorphic computing with physical model systems

Consider a simple physical model for the neuron's cell membrane potential *V*:



accelerated neuron model

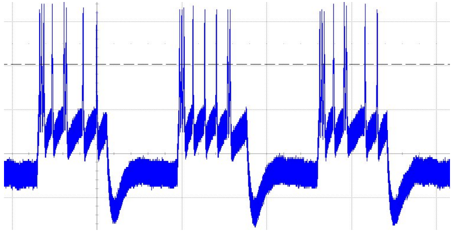


continuous time

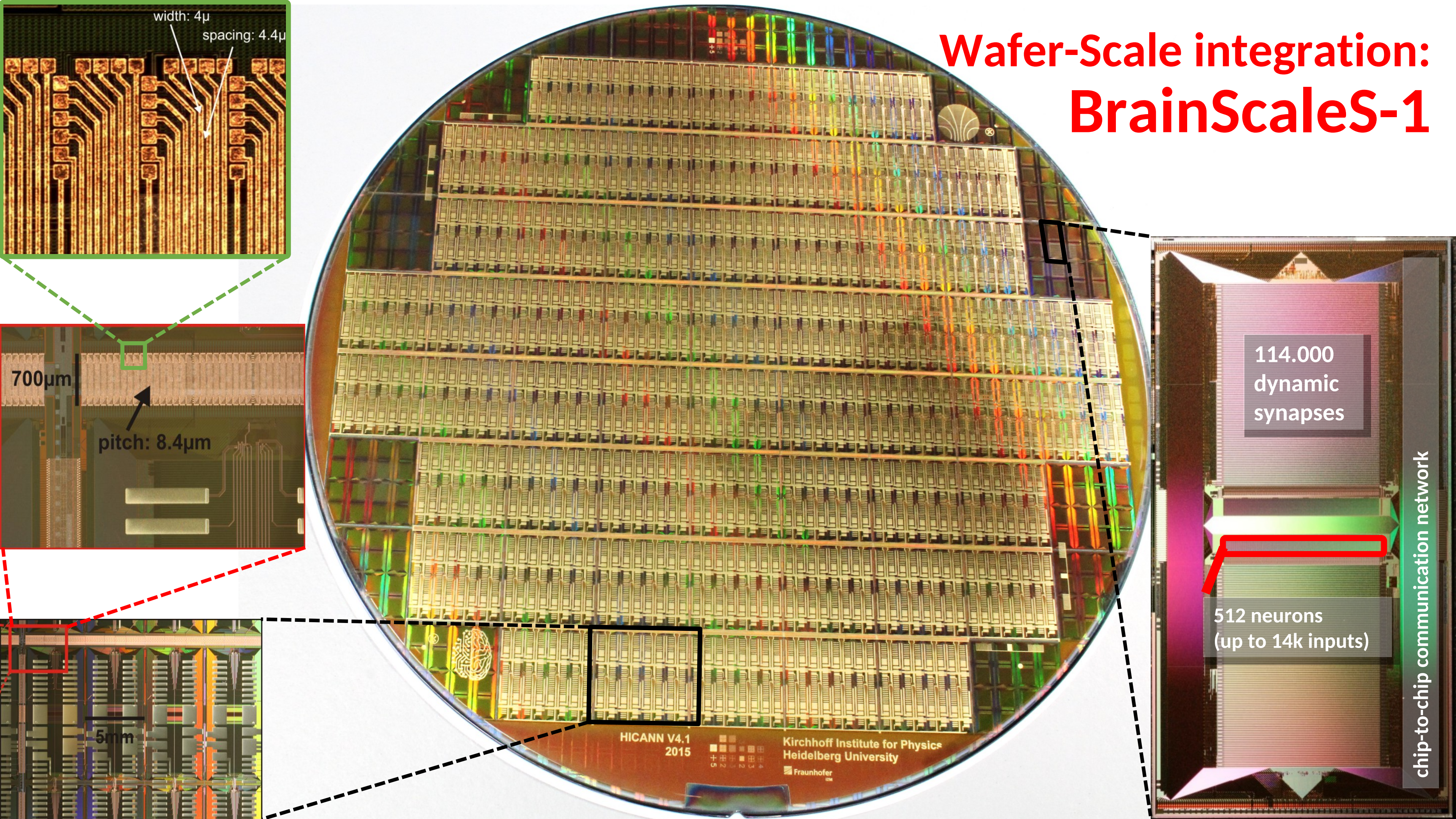
- fixed acceleration factor (we use 10^3 to 10^5)

no multiplexing of components storing model variables

- each neuron has its membrane capacitor
- each synapse has a physical realization

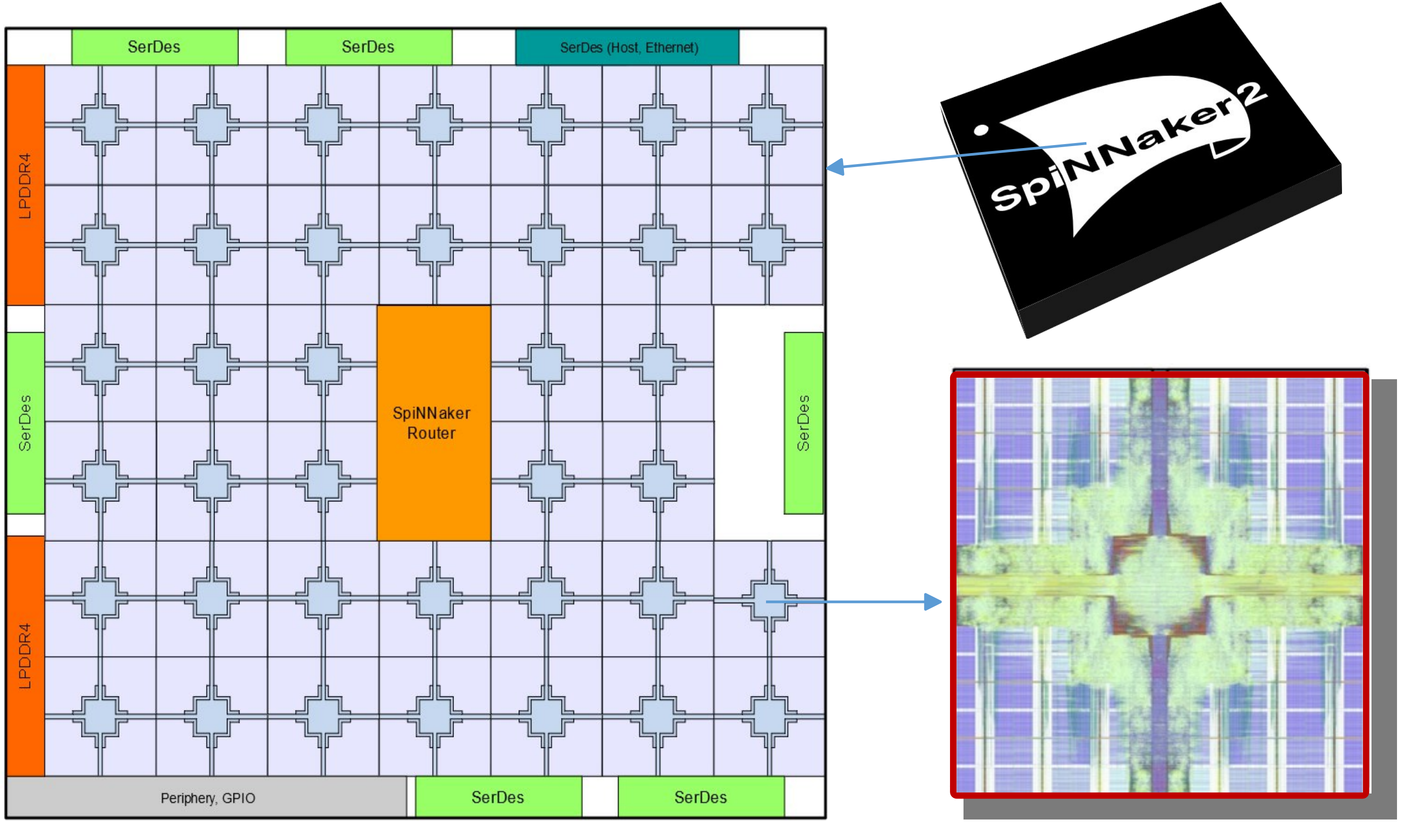


Wafer-Scale integration:
BrainScaleS-1

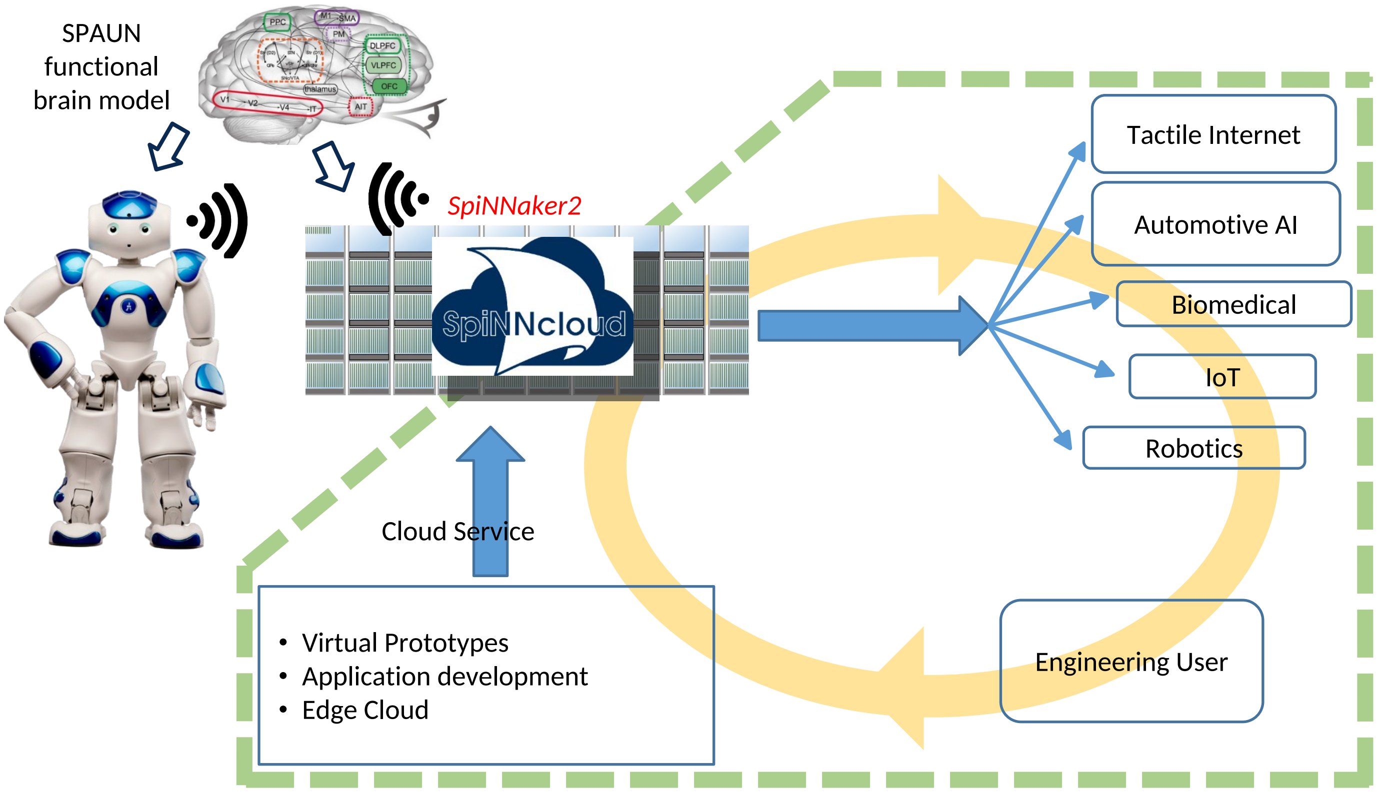


SpiNNaker-2

- 152 ARM-based processing elements
- 4 GByte DRAM
- 7 energy-efficient chip-to-chip links



SpiNNaker-2 in Dresden: SpiNNcloud



SPAUN
functional
brain model

SpiNNaker2

Cloud Service

- Virtual Prototypes
- Application development
- Edge Cloud

Tactile Internet

Automotive AI

Biomedical

IoT

Robotics

Engineering User

Use Model (Dresden): Edge Cloud for Tactile Internet

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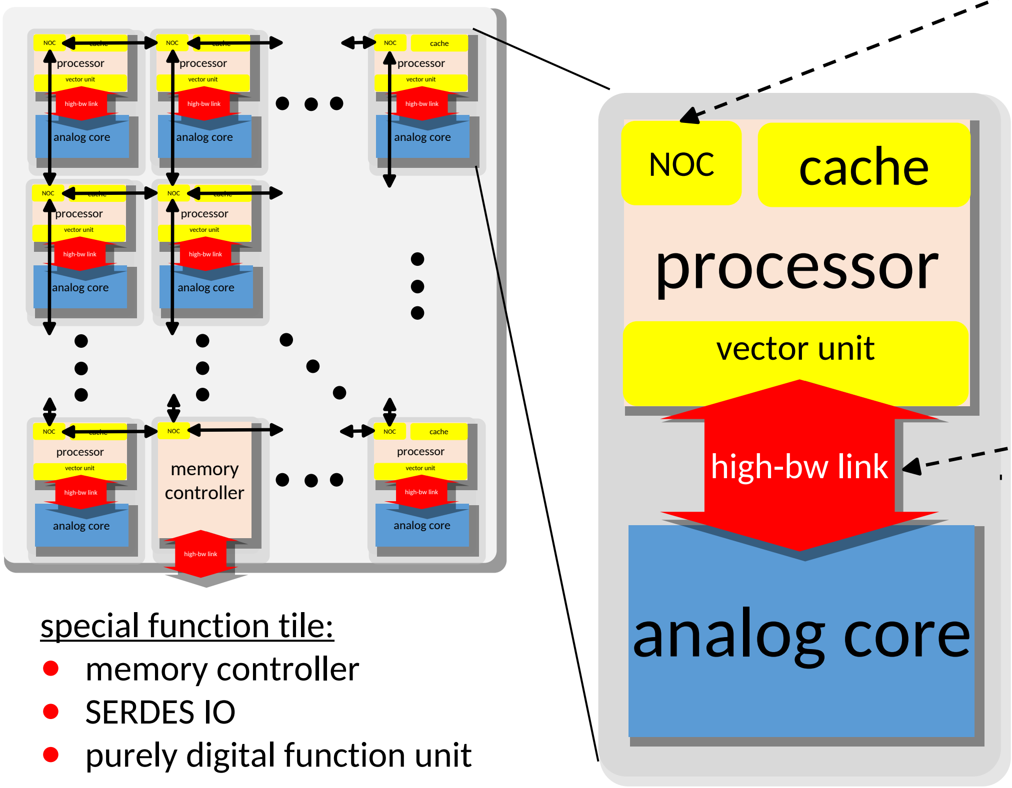
BrainScaleS-2: analog neuromorphic system as co-processor



Network-on-chip:

- prioritize event data
- unused bw for CPU
- common address space for neurons and CPUs

high-bandwidth link:

vector unit ≋ ☾ NM core

- weights
- correlation data
- routing topology
- event (spikes) IO
- configuration

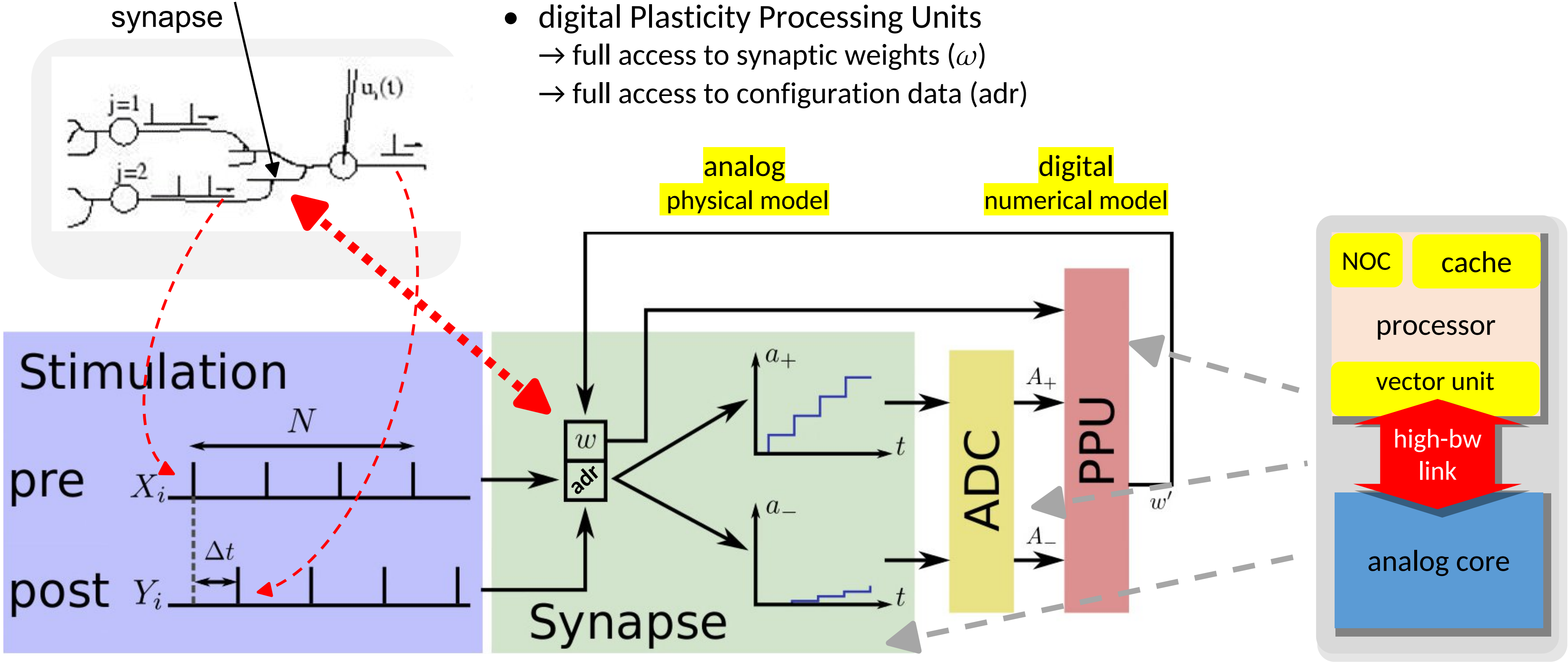
special function tile:

- memory controller
- SERDES IO
- purely digital function unit

BrainScaleS-2: implementing hybrid plasticity

- analog correlation measurement in synapses
- A/D conversion by parallel ADC
- digital Plasticity Processing Units
  → full access to synaptic weights (ω)
  → full access to configuration data (adr)

plasticity takes place at the synapse



n Brain Project

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NICE 2020

March 17 - 20th 2020

Neuro-Inspired Computational Elements Workshop

Im Neuenheimer Feld 227
D-69120 Heidelberg
Germany

Workshop: March 17-20th 2020
Tutorials: March 20th 2020

Heidelberg - Germany

Picture: fotolia.com / Sergey Borisov

Kirchhoff Institute for Physics

THANK YOU!

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